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# Role of non-uniform channel doping in improving the nanoscale JL DG MOSFET reliability against the self-heating effects

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ABSTRACT

In this paper, a new hybrid approach by combining numerical investigation and Support Vector Machines (SVMs) classifier is proposed to study the thermoelectric performance of nanoscale Double Gate Junctionless *DG JL MOSFET*. In this context, a new Figure of Merit (*FoM*) parameter which combines both electrical and reliability characteristics is proposed. Moreover, the impact of Gaussian channel doping profile (*GCD*) in enhancing the *DG JL MOSFET* reliability against the self-heating effects (*SHEs*) is presented. The proposed design thermal stability and electrical characteristics are investigated and compared with those of the conventional structure in order to reveal the device performance including SHEs. It is found that the amended channel doping has a profound implication in improving both the device electrical performance and the reliability against the undesired self-heating and short channel effects (*SCEs*). Furthermore, the transistor thermal behavior analysis involves classification of the device performance by taking into account the device reliability. For this purpose, *SVMs* are adopted for supervised classification in order to identify the most favorable design configurations associated with suppressed *SHEs* and improved electrical performance. We find that the proposed design methodology has succeeded in selecting the better designs that offer superior reliability against the *SHEs*. The obtained results suggest the possibility for bridging the gap between high electrical performances with better immunity to the *SHEs*.

## 1. Introduction

Nowadays, the continuous downscaling of the *MOSFETs* dimensions to follow Moore's law constitutes the key towards denser circuitry with improved functionality and high performance electronic chips [1]. However, when we go deeper into the sub-*50* nm regime, it becomes very difficult to control the elaboration of an ultra steep doping gradient at the device metallurgical junctions that imposes the high thermal budget [2]. In this regard, *MOSFETs* without metallurgical junctions at the source and drain sides called *JL* based-*FETs* were emerged as the most viable choice to avoid these experimental concerns. To this extent, the *DG JL MOSFET* demonstrates effective *SCEs* handling capability making it helpful for the future scaling

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