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MODELING AND SIMULATION OF THE ELECTRONIC AND OPTOELECTRONIC PROPERTIES OF CARBON NANOTUBES (APPLICATION TO C-CNTFET AND OG-CNTFET).

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2025/ 2026


بسم الله الرحمن الرحيم

Dedication

I sincerely dedicate this modest work to:

My beloved parents, ***LAOUAR Laid*** *and* ***Takouachet Fatima****.*

My beloved daughter, ***Sadjeda Li Allah****.*

My cherished brothers and sisters.

My dear husband.

I am deeply grateful to them for their unwavering belief in me, for enabling me to pursue and realize my dream, and for their trust even during moments of doubt. Their unconditional support and quiet presence throughout my journey have shaped who I am today. I wish to express that any achievement I have attained is fundamentally due to their encouragement and confidence.

To my entire family,

My respected teachers, colleagues, and friends,

And to all those who hold a special place in my life,

Thank you.

Hana

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General Introduction

The continuous advancement of nanoelectronics has intensified the demand for extreme miniaturization of electronic devices, driving the search for materials and technologies that can overcome the limitations of traditional silicon-based transistors. Silicon technology, which has dominated the semiconductor industry for decades, is approaching its fundamental physical and performance limits due to scaling challenges such as short-channel effects, increased power density, leakage currents, and emerging quantum phenomena at nanometer dimensions. These issues cause degradation in device reliability and energy efficiency, threatening the continuation of Moore's Law and the progress of integrated electronic circuits. To sustain and surpass current technological capabilities, exploring alternative materials and novel device architectures has become essential [1].

In this context, carbon-based nanomaterials especially carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) have gained significant attention as promising candidates for next-generation field-effect transistors (FETs). Their exceptional electrical, mechanical, and thermal properties, combined with atomic-scale thickness and one-dimensional or quasi-one-dimensional geometries, offer advantages that can potentially overcome silicon's limitations. The reduced dimensionality of these materials induces strong quantum confinement effects, resulting in tunable electronic band structures and enhanced carrier transport characteristics that are highly desirable for nanoelectronics applications [2].

Single-walled carbon nanotubes (SWCNTs) are cylindrical nanostructures formed by rolling a graphene sheet into a seamless tube with diameters typically in the range of one to a few nanometers. Their unique chirality-dependent electronic properties enable them to behave either as semiconductors or metals, providing flexibility for various device functionalities. Semiconducting CNTs demonstrate near-ballistic carrier transport over micrometer distances with minimal scattering, leading to transistor channels characterized by excellent current-voltage (I–V) performance and low power consumption. These features promise high-speed operation and energy-efficient switching, making CNTFETs attractive candidates for future nanoelectronics devices. However, several critical challenges remain, including achieving large-scale, uniform, and chirality-controlled synthesis of CNTs, precise alignment on substrates, and reliable device integration, which are active areas of research and development [3].

Graphene nanoribbons, narrow strips of graphene generally less than 50 nm wide, represent another class of carbon nanostructures with fascinating electronic properties. Unlike pristine graphene, which is gapless and thus unsuitable for digital switching applications, GNRs

exhibit finite and tunable bandgaps arising from quantum confinement and edge effects. The ability to open and tailor this bandgap is crucial for enabling efficient gate control of channel conductance and achieving high I_{on}/I_{off} ratios in transistor operation, overcoming the intrinsic limitation of graphene. Moreover, GNRs retain graphene's exceptional carrier mobility and thermal conductivity, combining high-speed transport with controllable electrostatics due to their narrow widths and atomically precise edges. Advances in fabrication techniques, including top-down lithography and bottom-up chemical synthesis (such as on-surface polymerization and solution-phase methods), have allowed for producing GNRs with well-defined width and edges, an essential step toward reproducible device performance and scalable applications [4].

Integrating CNTs and GNRs into field-effect transistor device architectures requires an interdisciplinary approach combining materials science, quantum physics, and electrical engineering. Carbon nanotube and graphene nanoribbon FETs offer promising pathways to address the scaling challenges faced by conventional silicon complementary metal–oxide–semiconductor (CMOS) technology, potentially providing improvements in switching speed, power efficiency, and device packing density. Furthermore, their intrinsic chemical robustness and compatibility with various substrates also open possibilities for flexible electronics, wearable devices, and chemical or biological sensing applications [5].

This thesis investigates two key directions within carbon-based nanoelectronics devices: the optoelectronic behavior of optical-gated CNTFETs (OG-CNTFETs) and the gas sensing performance of double-gated graphene nanoribbon FETs (DG-GNRFETs) employing $LaAlO_3$ as a high-k dielectric. The study of optical gating in CNTFETs probes how light illumination influences device I–V characteristics and induces photo-generated currents, providing insights into hybrid electrical-optical device operation. This approach leverages the unique interaction between CNTs and optical fields to achieve modulated transport properties, which could enable novel functionalities such as photo responsive switching and multi-modal sensing in nanoelectronics systems [6].

Simultaneously, the work explores how exposure to ammonia (NH_3) gas affects the electrical properties of DG-GNRFETs. NH_3 is a prevalent pollutant and environmental toxin; thus, reliable and miniaturized sensors capable of detecting it at low concentrations are highly desirable. The double-gate architecture offers enhanced electrostatic control over the GNR channel, improving the sensitivity and selectivity of the device to gas adsorption effects. The incorporation of $LaAlO_3$ as a high-permittivity dielectric improves gate coupling and reduces leakage currents, optimizing sensor performance. This investigation focuses on understanding

how various parameters such as gas concentration, gate voltage, dielectric thickness, and permittivity influence key device metrics like drain current modulation, I_{on}/I_{off} ratio, and transconductance, which are critical for evaluating sensor effectiveness [7].

The primary research questions guiding this thesis include: How does optical excitation modulate the I–V characteristics and carrier transport mechanisms in OG-CNTFETs? What impact does NH_3 exposure have on the electrical response and sensing capabilities of DG-GNRFETs with $LaAlO_3$ dielectric? How do device design parameters affect their optoelectronic behavior and gas sensing sensitivity? Addressing these questions advances both fundamental understanding and practical device optimization for emerging carbon-based nanoelectronics.

The structure of the thesis is as follows:

Chapter 1 provides an extensive overview of carbon allotropes, elucidating the atomic hybridization states and structural forms underpinning the diverse family of carbon nanomaterials. The chapter focuses primarily on CNTs and GNRs, dissecting their synthesis methods such as chemical vapor deposition (CVD), arc discharge, laser ablation for CNTs [8], and bottom-up solution-phase polymerization and on-surface synthesis for GNRs [9], the interplay between synthesis parameters, structural morphology, and intrinsic properties is critically analyzed, highlighting the prerequisites for optimizing device-grade materials.

Chapter 2 transitions into device fundamentals, initially discussing the working principles of generic field-effect transistors (FETs) and metal-oxide-semiconductor FETs (MOSFETs), emphasizing electrostatic control of the channel and scaling challenges. Building upon this foundation, the chapter explores CNTFETs in detail, categorizing their various types including single-walled, multi-walled, and double-gate configurations and surveying their superior transport characteristics and scalability prospects relative to silicon FETs. Special focus is given to optically gated CNTFETs (OG-CNTFETs), which introduce an optical control dimension, facilitating novel functionalities in sensing and reconfigurable logic [10].

Chapter 3 concentrates on graphene nanoribbon FETs (GNRFETs), delineating their fabrication routes, edge-dependent electronic properties, and device operation modes. It contextualizes GNRFET applications in nanoelectronics and sensing, underscoring ongoing efforts to engineer bandgaps through width control and edge termination for improved device performance [11]. The chapter evaluates future directions, including scalable production and integration in flexible electronics.

Chapter 4 presents a comprehensive theoretical and simulation study of OG-CNTFETs, analyzing the influence of optical excitation on device I–V characteristics. Key phenomena such as photocurrent generation dependence on optical power, wavelength, and effective illumination area are quantified. Comparative analyses of drain current under illuminated versus dark conditions at varying gate voltages are reported, offering critical insights into photo-induced charge modulation mechanisms for optoelectronic device applications.

Finally, Chapter 5 investigates gas sensing based on double gated GNRFETs under ammonia (NH_3) exposure, employing $LaAlO_3$ as a high-k gate dielectric. The study explores the impact of parameters including gas concentration, back-gate voltage, insulating layer thickness between graphene and gate electrodes, and dielectric permittivity on key metrics such as drain current modulation, I_{on}/I_{off} ratio, and transconductance. The outcomes illuminate optimization strategies for enhanced sensitivity and selectivity in nanoscale gas sensors [12].

Through rigorous modeling, simulation and theoretical investigations, this thesis aims to deepen understanding of carbon nanotube and graphene nanoribbon field-effect transistors, particularly their optoelectronic modulation and gas sensing capabilities. The ultimate goal is to contribute to the advancement of nano-carbon electronics from fundamental science to practical applications in sensing and optoelectronics, supporting the evolution of semiconductor technology beyond silicon and enabling innovative electronics that are faster, smaller, and more energy efficient.

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I. Introduction

Carbon, one of the most abundant and versatile elements on Earth, holds a foundational position in materials science due to its exceptional ability to form a wide spectrum of allotropes with highly distinct structural and physicochemical characteristics. These allotropes range from traditional three-dimensional forms such as diamond and graphite to novel low-dimensional nanostructures, including fullerenes, carbon nanotubes (CNTs), and graphene, each exhibiting unique properties that have propelled significant research and technological advancements [1,2]. This chapter offers a comprehensive overview of these carbon allotropes, emphasizing their structural diversity and the intrinsic properties that render them indispensable in contemporary nanotechnology and electronic applications.

Special focus is placed on carbon nanotubes, whose cylindrical graphene-based architecture endows them with exceptional mechanical strength, electrical conductivity, and thermal stability, making them crucial for nanoelectronic devices and advanced composite materials [3,4]. Advances in synthesis techniques, particularly chemical vapor deposition (CVD), laser ablation, and arc discharge, have been pivotal in tailoring CNT properties, addressing challenges of controlled growth, purity, and yield [5,6].

The discussion naturally progresses to graphene nanoribbons (GNRs), a promising class of carbon nanomaterials defined by their narrow width and edge-dependent electronic properties. GNRs offer tunable bandgaps induced by quantum confinement, overcoming the intrinsic zero bandgap limitation of graphene and thereby enabling their application in transistor and optoelectronic device technologies [7,8]. The structural precision of GNRs, achievable through lithographic patterning, chemical synthesis, and unzipping of CNTs, is critical for their electronic behavior, as even atomic-scale variations in edge morphology can drastically alter their band structure [9,10]. By systematically examining the properties, synthesis methodologies, and applications of CNTs and GNRs, this chapter establishes a solid theoretical framework integral to advancing the understanding and development of graphene-based nanostructures. These insights provide the essential background for the detailed experimental and modeling investigations presented in subsequent chapters, contributing to the expanding landscape of carbon nanomaterials and their integration into next-generation technologies.

I.1 Carbon

Carbon is a fundamental element of life and possesses a remarkable ability to form diverse bonds with a wide variety of other atoms, enabling an extensive array of synthetic

possibilities. This versatility arises from its unique electronic configuration, $1s^2\ 2s^2\ 2p^2$, which allows its atomic orbitals to hybridize in several ways. Carbon atoms can achieve sp^1, sp^2, or sp^3 hybridization by combining orbitals with those of other carbon atoms or heteroatoms. As a result, carbon can exhibit bi-, tri-, or tetravalency, leading to the formation of one-dimensional, two-dimensional, or three-dimensional carbon-based structures. Among all allotropes, only hexagonal graphite is thermodynamically stable under standard conditions of temperature and pressure. Other carbon allotropes, such as diamond, amorphous carbon, and recently discovered structures including fullerenes, multi-walled carbon nanotubes, and single-walled carbon nanotubes are considered metastable phases. These new carbon forms expand the traditional understanding of carbon's structural diversity and have opened new avenues for research in materials science [11].

I.1.1 Allotropic Forms of Carbon

Carbon is renowned for its ability to form a remarkable variety of allotropes and structural forms in which atoms bond in distinct patterns, resulting in dramatically different physical and chemical properties [12]. This versatility arises from the capacity of carbon atoms to undergo different hybridizations sp^1, sp^2, and sp^3 enabling a range of molecular geometries and materials, from ultra-hard diamonds with sp^3 bonds [13] to nanostructures like fullerenes [14] and graphene with sp^2 bonding [15]. Such diverse bonding configurations form the basis for the exceptional mechanical, electrical, and thermal properties exhibited by these carbon allotropes [16]. **Figure I.1** illustrates representative nanostructured allotropes of carbon categorized by their dimensionality: zero-dimensional (0D), one-dimensional (1D), two-dimensional (2D), and three-dimensional (3D) forms. This classification visually communicates the extraordinary structural diversity of carbon, from 0D fullerenes and carbon dots, through 1D carbon nanotubes, 2D graphene sheets, to 3D diamond and graphite structures, each with unique chemical bonds and physical attributes critical to their various applications.

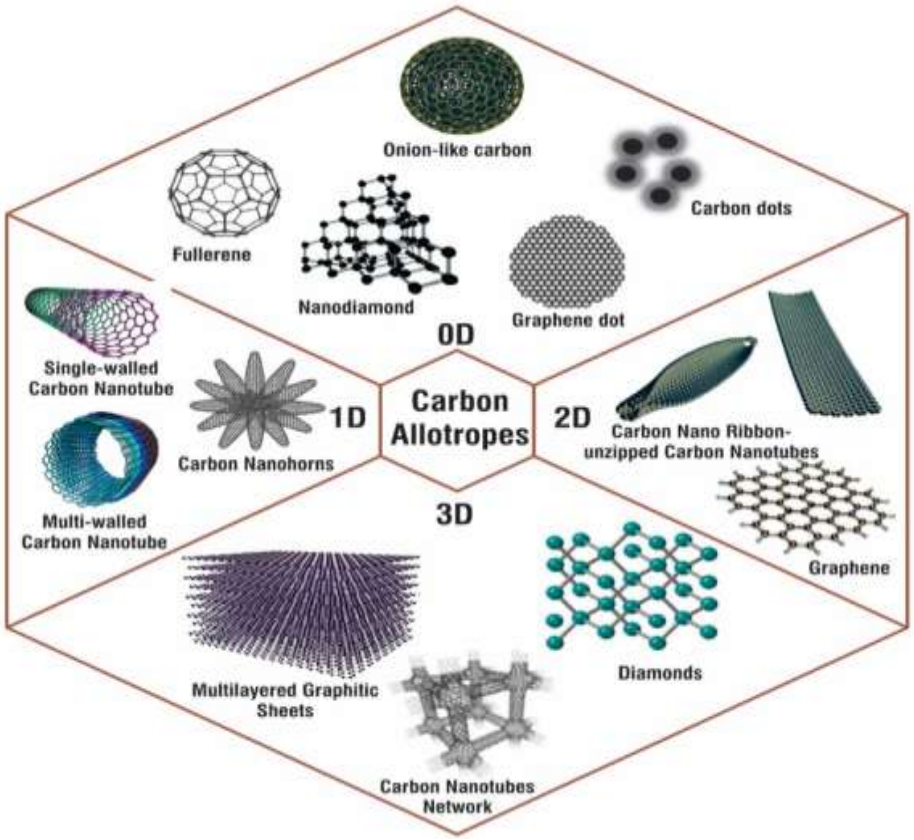


Figure I.1. *Representative nanostructured allotropes of carbon, illustrating examples in: zero-dimensional (0D), one-dimensional (1D), two-dimensional (2D), and three-dimensional (3D) category forms [17].*

I.1.1.1 Classical Allotropes

I.1.1.1.1 Diamond

Diamond is a transparent material known for its exceptional hardness and density, composed entirely of carbon atoms arranged in a specific three-dimensional structure [18,19]. It is important to emphasize that natural diamond formation requires extreme conditions, with temperatures above 1000 °C and pressures reaching several Giga-pascals [18,20]. Within the diamond crystal lattice, each carbon atom adopts sp^3 hybridization state, which imparts tetravalency, allowing each atom to form covalent bonds with four neighboring carbon atoms in a tetrahedral geometry [21,22].

From a crystallographic structure, diamond's structure is derived from the face-centered cubic (FCC) lattice, commonly referred to as the diamond cubic structure [23]. This arrangement involves a spatially repetitive pattern where, in addition to carbon atoms located at the cube's corners and face centers, four atoms occupy specific tetrahedral sites within the

unit cell [20,23], resulting in eight atoms per unit cell. The bond length between adjacent carbon atoms is approximately 1.54 À, and the strong, short covalent bonds contribute to the material's remarkable rigidity and hardness [19,21]. Diamond's hardness is also influenced by crystal perfection, purity, and crystallographic orientation, with the greatest hardness typically observed along the <111> direction, which corresponds to the longest diagonal of the cubic unit cell [19,24]. While the cubic form of diamond is the most common, rare forms such as hexagonal diamond (lonsdaleite) can form under even more extreme conditions, such as meteorite impacts, and exhibit slightly different mechanical properties [18,25]. However, the most prevalent and extensively observed structure is the cubic diamond (**Figure I.2**). This particular form features a face-centered cubic (FCC) lattice with a lattice parameter of 0.356 nm and an interatomic spacing of 0.154 nm [26].

Diamond is an exceptionally durable material with a wide range of applications. At room temperature, it exhibits the highest thermal conductivity of all known solid materials, making it highly effective for heat dissipation [27,28]. Additionally, diamond can be doped with trace amounts of various elements such as lithium, boron, nitrogen, or phosphorus, which enables it to function as a semiconductor [29,30]. Furthermore, diamond has a high refractive index that efficiently transmit light across a broad spectrum, from the far infrared to the ultraviolet range [31,32].

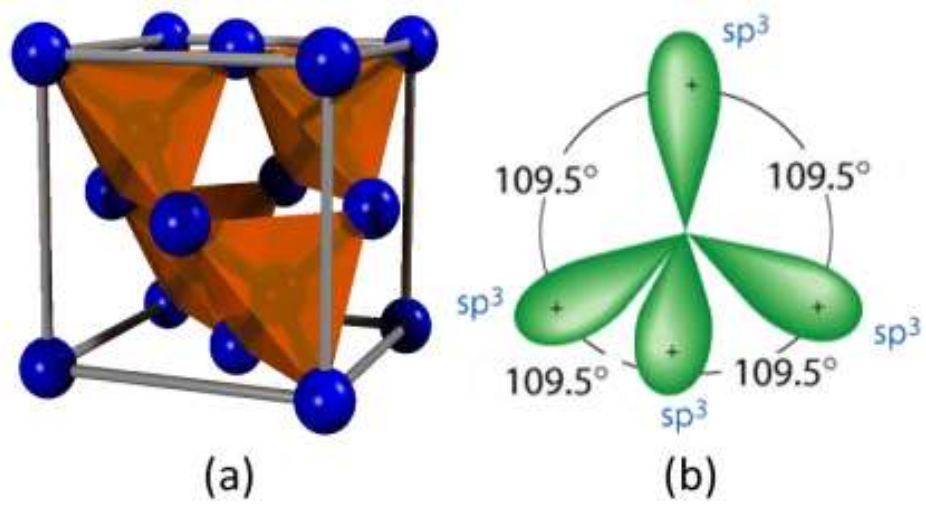


Figure I.2. *Crystallographic representation of the diamond structure, (b) depiction of the four atomic orbitals of sp³-hybridized carbon atom [33].*

I.1.1.1.2 Graphite

Graphite possesses a lamellar structure composed of carbon atoms arranged in a hexagonal lattice, often described as a honeycomb pattern, where adjacent graphene layers are spaced approximately 3.35 Å apart (**Figure I.3**). Within each plane, carbon atoms are bonded through strong covalent bonds, while the planes themselves are held together by weak van der Waals interactions. These weak interlayer forces enable easy cleavage of graphite layers, which facilitates the deposition of graphite onto surfaces by friction thus allowing it to be used as pencil "lead." The ability of graphene layers to slide over each other also accounts for graphite's widespread use as a solid lubricant.

Important research efforts have been devoted to isolating single graphene sheets from graphite [34–36], exploiting its weak interlayer bonding. Notably, the synthesis of a bilayer graphene structure was first reported in 2006, marking a crucial step in graphene research and applications [37].

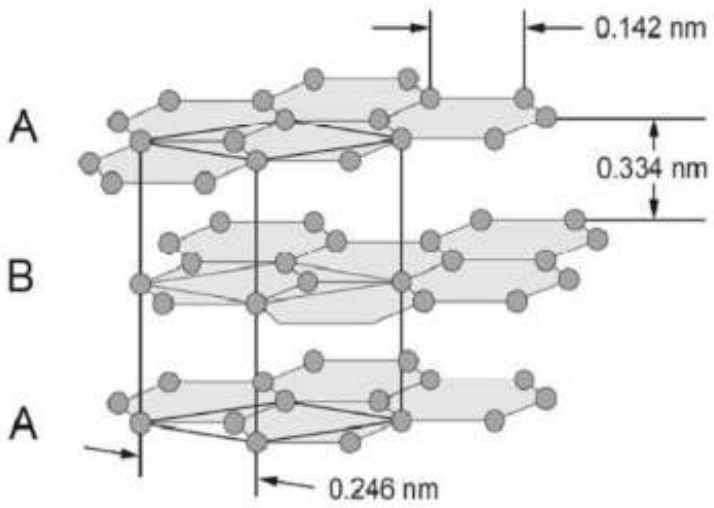


Figure I.3. *Hexagonal crystal structure of graphite [38].*

I.1.2 Molecular and Nanoscale Allotropes

I.1.2.1 Fullerenes

Fullerenes constitute a distinct category of carbon allotropes formed by the closure of curved graphene sheets into cage-like structures. For example, highly stable fullerenes typically emerge when the system contains fewer than a few hundred carbon atoms, as first demonstrated

in the case of C_{60} [39]. In a landmark experiment conducted in 1985, Harold et al. Smalley, and Robert Curl [40] succeeded in isolating a particularly symmetrical molecule built from exactly 60 carbon atoms Buckminsterfullerene (C_{60}). This molecule displays a truncated icosahedral geometry, analogous to a soccer ball or geodesic dome: it has 12 pentagonal and 20 hexagonal faces, with one carbon atom located at each of the 60 vertices. This configuration results in exceptional structural stability as well as notable electronic and optical properties, rendering C_{60} a prototype for a wider class of carbon nanostructures.

Recent research has elucidated several novel physical and chemical properties of C_{60}, especially for molecules synthesized via electric arc discharge. Notably, the structure can be described in terms of two different C–C bonds: the "6–6" bonds, which are shared between two adjacent hexagons and exhibit significant double-bond character, and the "5–6" bonds, which link a pentagon and a hexagon and are comparatively longer and weaker due to geometric constraints. These subtle variations in bonding play a crucial role in dictating the reactivity and electronic characteristics of the molecule.

The synthetic versatility of the fullerene structure has enabled the expansion of the family to larger homologues. For instance, by incrementally inserting additional rings of carbon atoms and delaying the final shell closure, researchers have prepared elongated fullerene cages such as C_{70} which features 25 hexagons and 12 pentagons and even larger species like C_{80}, which possesses 30 hexagons and 12 pentagons [41]. Each larger fullerene retains the fundamental closed-cage topology but exhibits symmetry and properties distinct from those of C_{60} [42,43]. Moreover, these fullerene structures serve as building blocks for advanced materials and have catalyzed significant progress in multiple areas, including organic photovoltaics, drug delivery systems, and molecular electronics [44-46]. The study of their topological, electronic, and functional diversity continues to push the boundaries of both organic and inorganic chemistry, opening new realms for synthesis and application [47,48]. This structural evolution is well illustrated in **Figure I.4**, which shows (a) a high-resolution transmission electron microscopy (HRTEM) image of pristine C_{60}, capturing the iconic spherical topology, and (b) a model depicting the addition of carbon atoms (highlighted in orange) to the C_{60} fullerene framework, resulting in the formation of the larger C_{70} and C_{80} fullerenes with their extended cage structures. These visualizations underscore the incremental expansion principle underlying fullerene synthesis and help contextualize their increasing complexity and functional diversity.

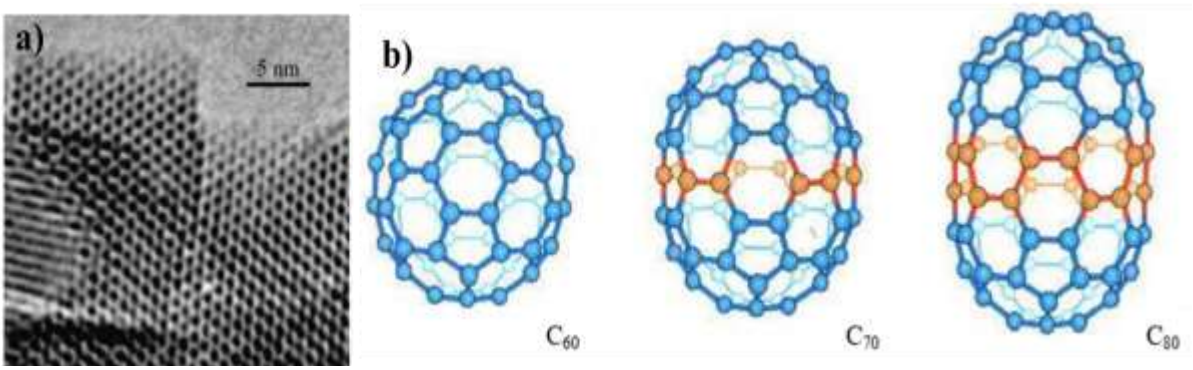


Figure I.4. *a) High-resolution transmission electron microscopy (HRTEM) image of pristine C_{60} [49]. b) Addition of carbon atoms (highlighted in orange) to the C_{60} fullerene structure, resulting in the formation of larger fullerenes C_{70} and C_{80} [50].*

I.1.2.2 Carbon Nanotubes (CNTs)

CNT were first discovered and characterized in 1991 by Sumio Iijima [3], marking a pivotal moment in nanoscience. Nonetheless, their unintentional manufacture dates back much earlier; for example, carbon nanotubes were found in Damascus swords fabricated in the 17th century [51,52]. Structurally, a carbon nanotube can be viewed as a graphene sheet rolled into a cylindrical form with diameters typically on the nanometer scale. The ends of these tubes are generally capped by hemispherical fullerene-like structures [53,54]. Another way to conceptualize a nanotube is to start from a fullerene molecule and extend it lengthwise by adding successive rings of carbon atoms [53], resulting in a tube wall composed entirely of hexagonal carbon rings. Except for the end caps, which resemble fullerene geometry, a carbon nanotube predominantly features sp^2 hybridized carbon structure. However, due to the curvature of the tube, there is a degree of sp^3 hybridization, which increases as the tube diameter decreases [55]. They stand out for their incredible mechanical strength, elasticity, high electrical and thermal conductivities, and flexibility [56, 57]. Their diverse uses span electronics (e.g., transistors, sensors, batteries) [58, 59], composite materials (enhancing strength while remaining lightweight) [60], medicine (drug delivery, biosensors) [61,62], water purification [63], and nanorobotics [64]. **Figure I.5** presents a transmission electron microscopy (TEM) image illustrating a bundle of single-walled carbon nanotubes (SWNTs). Each circle indicates an individual SWNT with a diameter of about 1.4 nm, visualizing the nanoscale cylindrical structure of these graphene-based tubes.

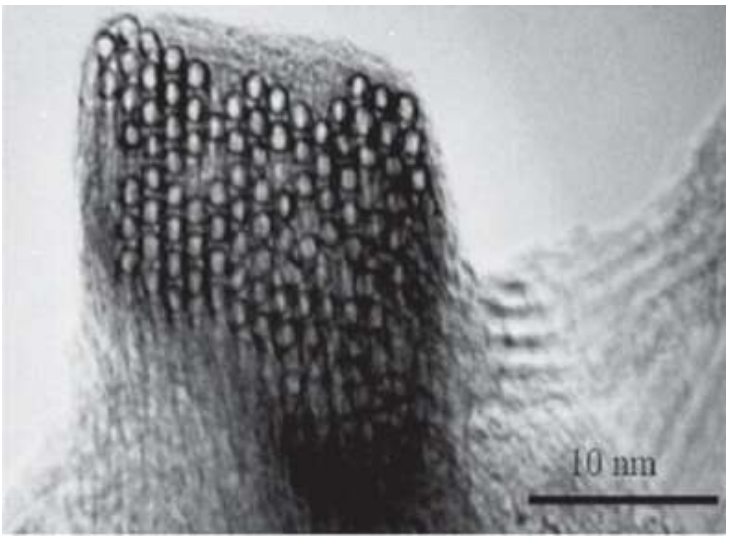


Figure 1.5. *TEM image of a bundle of single-walled carbon nanotubes (SWNTs), with each circle indicating an individual SWNT having a diameter of about 1.4 nm [65].*

I.1.2.3 Graphene

In 2004, graphene was successfully isolated for the first time by the distinguished scientists A. Geim and K. Novoselov at the University of Manchester. Their pioneering experiments fundamentally transformed carbon nanoscience and earned them the Nobel Prize in Physics in 2010, honoring the significance of their discovery to the broader scientific community. Before this experimental breakthrough, graphene had been understood primarily as a theoretical construct, representing the fundamental structure underlying graphite. The identification of graphene as an independent material established it as the fifth known allotropic form of carbon. Currently, graphene is recognized alongside graphite, fullerenes, and carbon nanotubes as prominent carbon allotrope.

Graphene's remarkable properties originate from the unique arrangement of its carbon atoms, where sp^2-hybridized carbon atoms are arranged in a densely packed honeycomb lattice, forming a two-dimensional atomic-scale structure (Figure I.6). This atomic-scale arrangement within the graphene sheet underpins its exceptional electrical, mechanical, and thermal characteristics, making it a foundational material in the field of nanotechnology.

Graphene consists of a single atomic layer of carbon atoms tightly packed into a bipartite honeycomb lattice. Each carbon atom is bonded to three nearest neighbors via strong covalent sp^2 bonds with a C–C bond length of approximately 1.42 Å, while the fourth electron forms a delocalized π-bond perpendicular to the plane [15,68]. This atomically thin sheet, usually considered as two-dimensional (2D), has a thickness of around 0.34 nm, essentially the diameter

of a carbon atom [68]. The hexagonal unit cell contains two inequivalent carbon atoms with unique electronic band structures and Dirac cones at K and K′ points in the Brillouin zone. This structure leads to quasi-relativistic charge carriers exhibiting linear energy dispersion near these Dirac points displays a remarkable Mechanically, properties [15,69,70].

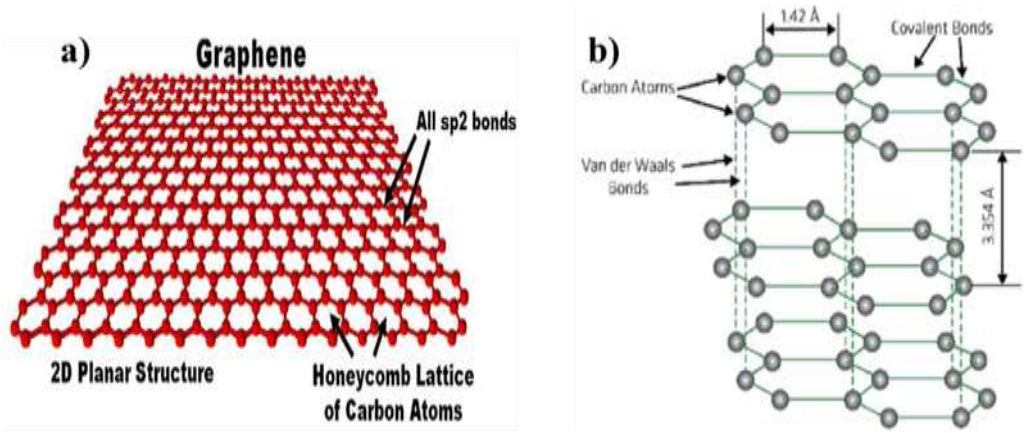


Figure I.6. *Graphene structure illustrating: (a) sp²-hybridized carbon atoms arranged in a densely packed honeycomb lattice; (b) the atomic-scale arrangement of carbon atoms within graphene sheet [66,67].*

Figure I.7 provides a detailed atomic-level visualization of this bonding configuration: (a) depicts the sp² hybrid orbitals localized on an individual carbon atom, demonstrating the planar nature of these orbitals, while (b) illustrates how these sp² orbitals engage in covalent bonding with adjacent carbon atoms, forming the robust honeycomb lattice characteristic of graphene.

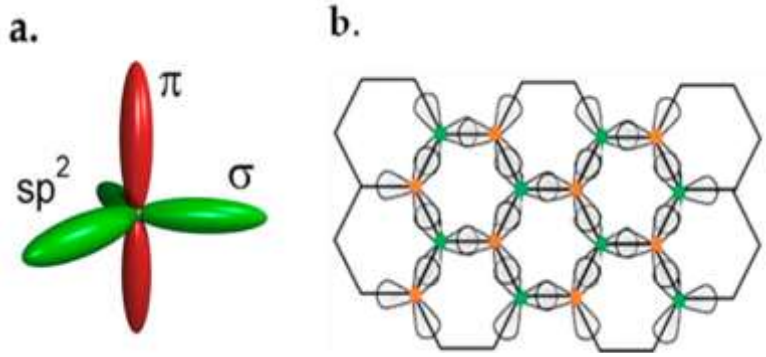


Figure I.7. *(a) Visualization of the sp² hybrid orbitals localized on an individual carbon atom [71]. (b) Depiction of the sp² hybrid orbitals of a carbon atom engaged in covalent bonding with adjacent carbon atoms [72].*

I.1.2.4 Carbon Nanofoam

Carbon nanofoam is a highly porous, extremely lightweight form of carbon having a density of ~2 mg/cm^3, with a unique three-dimensional network of graphite-like clusters [73,74]. Unlike other allotropes, nanofoam exhibits unusual magnetic properties (ferromagnetism), low density, high surface area, and excellent electrical insulation [75,76]. These characteristics make it suitable for energy storage, specialty optics, filtration, and advanced composite materials, as well as various scientific and battery technologies [77,78]. **Figure I.8** presents helium-ion microscopy (HIM) images illustrating the morphology of carbon nanofoams with differing densities. Panels (a) and (b) display low-density nanofoam structures at varying magnifications, whereas panels (c) and (d) show corresponding high-density nanofoams under different magnifications. Panel (e) depicts a nanofoam with a porosity of 50% and an sp^3 content of 49.1%, as indicated in the inset, which illustrates the hybridization states of the carbon atoms on the foam filaments. These images underscore the structural diversity and hybridization characteristics that underlie the remarkable physical and chemical properties of carbon nanofoams and their promising technological applications. **Figure I.8** displays helium-ion microscopy (HIM) images that illustrate structural differences in carbon nanofoams with varying densities. These microscopy images capture the microstructural evolution across density regimes, offering insights into the interplay between sp^2 and sp^3 hybridizations that underpin nanofoam's exceptional physical and chemical behaviors, which in turn inform its promising technological applications.

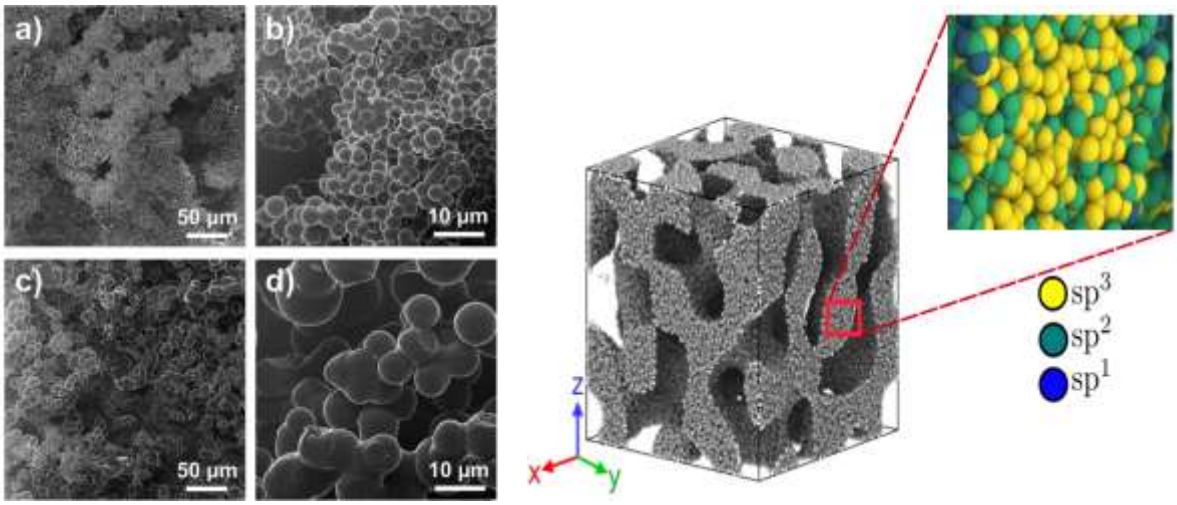


Figure I.8. *Helium-ion microscopy (HIM) images illustrating the morphology of carbon nanofoams with differing densities. Panels (a) and (b) display low-density nanofoam structures at varying magnifications, while panels (c) and (d) show high-density nanofoams at different magnification levels [79], (e)Nanofoam with a porosity of 50% and an sp3 content of 49.1%. Inset shows the hybridization of the C atoms on the foam filaments [80].*

I.1.3 Hybrid and Novel Allotropes

Ongoing studies have discovered new forms of carbon allotropes that incorporate both sp^2 and sp^3 bonding configurations. One such allotrope, known as HSH-carbon, is a designed structure that exhibits a combination of these hybridizations. This unique bonding arrangement imparts distinct electronic bandgaps, density, and mechanical characteristics, making HSH-carbon a promising candidate for applications including molecular separation technologies and future semiconductor devices [81-83].

I.1.4 The Role of Hybridization and Structural Motifs

The vast variety of carbon allotropes arises primarily from the different ways carbon atoms hybridize sp^1, sp^2, and sp^3 which determine their dimensionality (ranging from zero-dimensional to three-dimensional structures), electronic band structures, and resulting physical properties [43,84]. Graphene serves as a fundamental structural unit, acting as a versatile "building block": it can be rolled to form one-dimensional carbon nanotubes, folded into zero-dimensional fullerenes, or stacked in multiple layers to construct two-dimensional or three-dimensional graphite **Figure I.9** visually illustrates these allotropes, showing zero-dimensional fullerenes as closed spheres, one-dimensional carbon nanotubes formed by rolling graphene into cylinders, and three-dimensional graphite created by stacking layers [85,15].

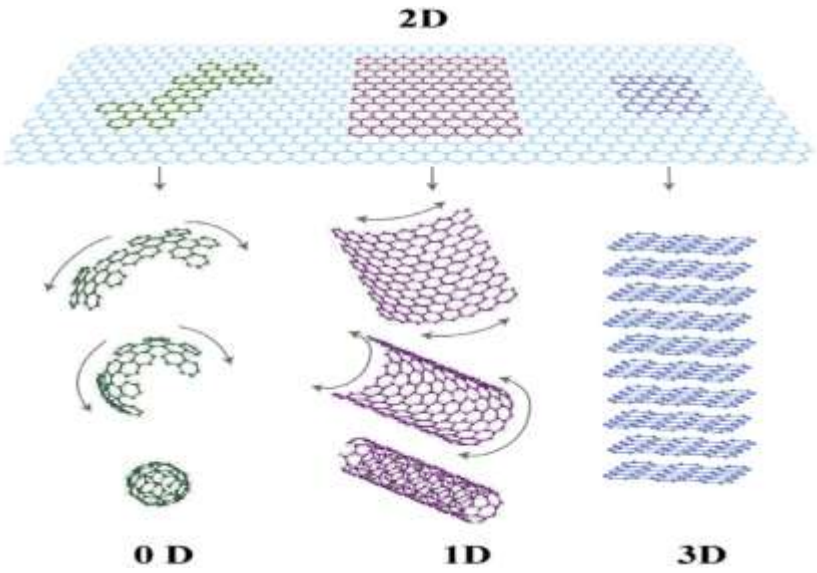


Figure I.9. *Various carbon allotropes: zero-dimensional fullerenes by closing into spheres, one-dimensional carbon nanotubes by rolling into cylinders, and three-dimensional graphite through stacking of layers [85].*

Computational methods, particularly Density Functional Theory (DFT), have become critical tools in advancing our understanding of these carbon materials by accurately predicting their stability, mechanical properties, and electronic characteristics, both for traditional allotropes and for novel, engineered carbon structures [86,87]. Carbon exists in various allotropes, each exhibiting unique structures and properties that lend themselves to diverse commercial and laboratory applications. **Table I.1** summarizes these forms of carbon, highlighting their distinctive characteristics and typical uses. Understanding these applications underscores the critical roles carbon allotropes play across scientific research and industrial sectors, from electronics and biotechnology to materials science and energy storage.

Table I. 1. *Various forms of carbons and their commercial and laboratory application.*

Carbonaceous Materials	Structural Design	Presence in Environment and Popular Synthesis Method	Applications	Ref.
Carbon Nanotubes	1D tubular sp^2	Arc discharge, Laser ablation, Chemical Vapor Deposition	Biosensors, nanocomposite materials as scaffolds for tissue engineering.	[88,89]
Fullerenes	0D cage-like sp^2	Manufactured at large scale in industry and laboratory. Chemical Vapor Deposition	Pharmaceutical industry. Found to be beneficial in IT devices and diagnostic purposes.	[90]
Carbon Nanofoam	3D porous sp^2	Study of porous carbon structures, magnetic materials	Energy storage, filtration, specialty materials	[91,92]
Diamond	3D, sp^3 hybridized	Can be obtained naturally or by artificial means. Rapid pressurisation, pulsed laser ablation	Used as lubricant in higher temperature. Used in jewellery design, biomedical etc.	[93–95]
Graphene	2D monolayer sp^2	Obtained by artificial means through laboratory production Arc discharge, chemical vapor deposition, mechanical exfoliation	Biosensing, bioimaging, bone implantation, drug delivery.	[96,97]
Graphite	3D layered, sp^2	Laboratory and industrial production can be obtained through natural process.	Mechanical heart valves, electrode components, lubricants.	[98]

I.2. Carbon Nanotubes

The entire development of carbon nanotubes truly began in 1993, when a group of Japanese researchers, led by Iijima and Bethune at NEC in Tsukuba, Japan, identified hollow

cylindrical carbon molecules now known as single-walled carbon nanotubes (SWCNTs). These structures were obtained by electron microscopy in a by-product of fullerene synthesis [99,100]. The nanotubes detected are spaced about 0.34 nm apart, with diameters of nanometers order and lengths reaching several micrometers. **Figure I.10** presents electron micrographs of CNTs, showing (A) a scanning electron microscopy (SEM) image illustrating the surface morphology of CNTs, and (B) a transmission electron microscopy (TEM) image revealing detailed internal structural information. Since this discovery, various targeted synthesis methods have been developed, enabling the laboratory study of these nanotubes and their unique physicochemical properties. These advances open the door to numerous potential applications, particularly in microelectronics. Furthermore, it is noteworthy that some carbon nanotubes exhibit metallic or quasi-metallic behavior, while others act as semiconductors, significantly broadening their range of applications.

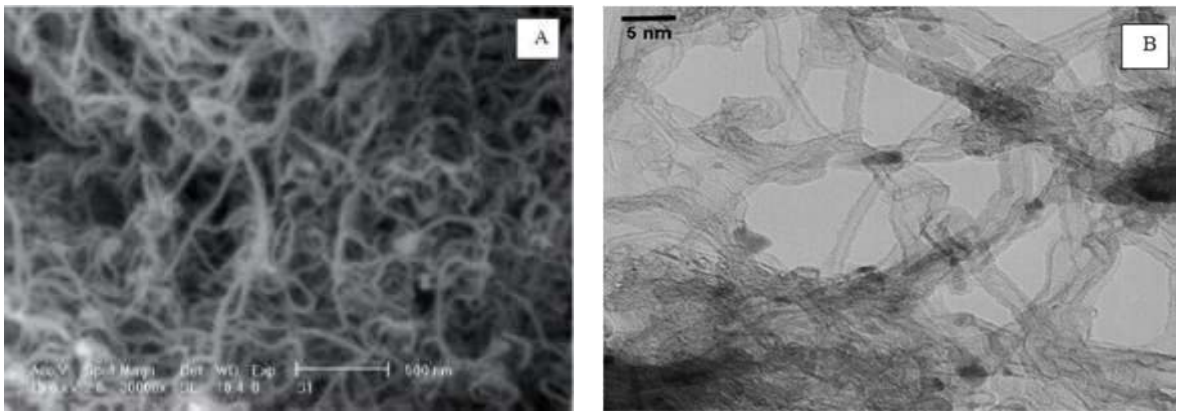


Figure I.10. *Electron micrographs of CNT (A) SEM of the CNT, (B) TEM of the CNT [101]*

I.2.1 Physical Properties of Carbon Nanotubes

I.2.1.1 Geometric Structure

Carbon nanotubes (CNTs) are broadly categorized into two distinct electronic types: metallic and semiconducting. Metallic CNTs exhibit electrical conductivity akin to metals, whereas semiconducting CNTs display properties characteristic of semiconductor materials. These electronic properties render CNTs highly promising for a diverse range of advanced applications, particularly as active components in nanoelectronics devices or as nanoscale interconnects within integrated systems [102]. In the present work, focus is restricted exclusively to semiconducting carbon nanotubes due to their relevance in the targeted research

domain. From a structural perspective, carbon nanotubes are further classified based on the number of concentric graphene layers they comprise. Single-walled carbon nanotubes (SWCNTs) consist of one graphene cylindrical layer, while multi-walled carbon nanotubes (MWCNTs) are composed of multiple nested graphene cylinders. Situated between these two classes are double-walled carbon nanotubes (DWCNTs), possessing two coaxial graphene walls, which combine certain properties of both SWCNTs and MWCNTs. This classification is critical, as structural differences influence the electronic, mechanical, and chemical behaviors of CNTs, thereby impacting their functional applicability in nanotechnology and materials science. Figure I.11 illustrates the different structural types of carbon nanotubes.

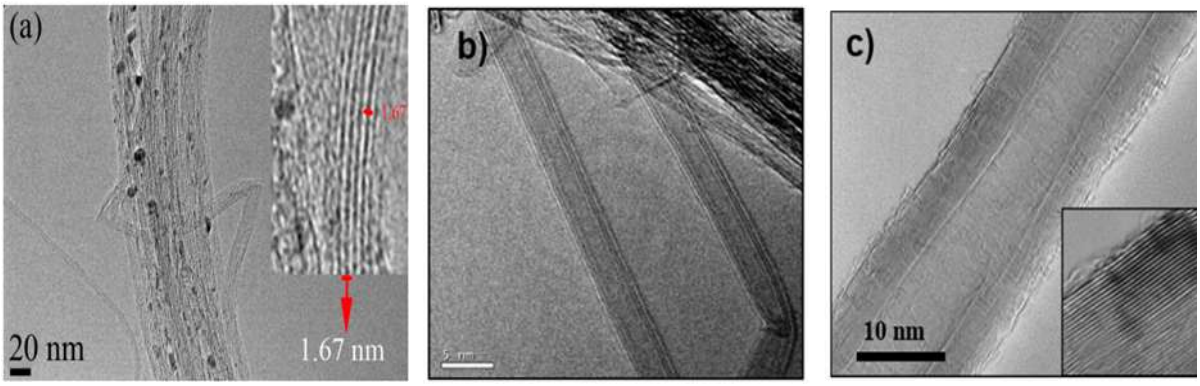


***Figure I.11**. Carbon nanotubes: a) single-walled (SWCNT) [103], b) double-walled, c) multi-walled (MWCNT) [104].*

a) Single-walled Carbon Nanotubes (SWCNTs)

A single-walled carbon nanotube (SWCNT) can be conceptualized as a stable graphene sheet rolled seamlessly into a cylindrical shape. The geometry of this nanotube is characterized by a pair of integers, (n, m), which define a unique vector known as the chirality vector. This vector specifies the direction and manner in which the graphene sheet is wrapped to form the nanotube structure [105,106].

$$C_h = n\overrightarrow{a_1} + m\overrightarrow{a_2} \qquad \text{(I.1)}$$

The vectors $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$ are the so-called unit base vectors of the hexagonal lattice.

Knowing that the distance a_{c-c}between two neighboring carbon atoms is approximately $0.142nm$, we have $\|\overrightarrow{a_1}\|=\|\overrightarrow{a_2}\|$=0,246 nm. Thus, the diameter of the nanotube, in nanometers, is expressed as:

$$d_{CNT} = 0{,}246 * \frac{\sqrt{n^2+m.n+m^2}}{\pi} \quad \text{(I.2)}$$

The helicity angle θ, which describes the curvature of the graphene sheet, can be defined as follows [107]:

$$\theta = \arctan\left(\frac{\sqrt{3m}}{m+2n}\right) \qquad (I.3)$$

The classification of single-walled carbon nanotubes (SWCNTs) is determined by the value of the helicity angle θ, which ranges between 0° and 30°. In practice, most nanotubes are statistically chiral, meaning they are superimposable on their mirror images by symmetry. However, other nanotubes exhibit distinctive symmetries. Specifically, tubes are referred to as "armchair" (**Figure I.12**) when the helicity angle θ equals 30°, which corresponds to chirality indices where n = m (i.e., (n, n)) [108].

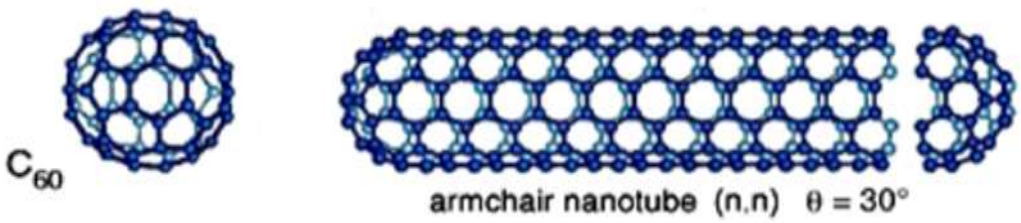
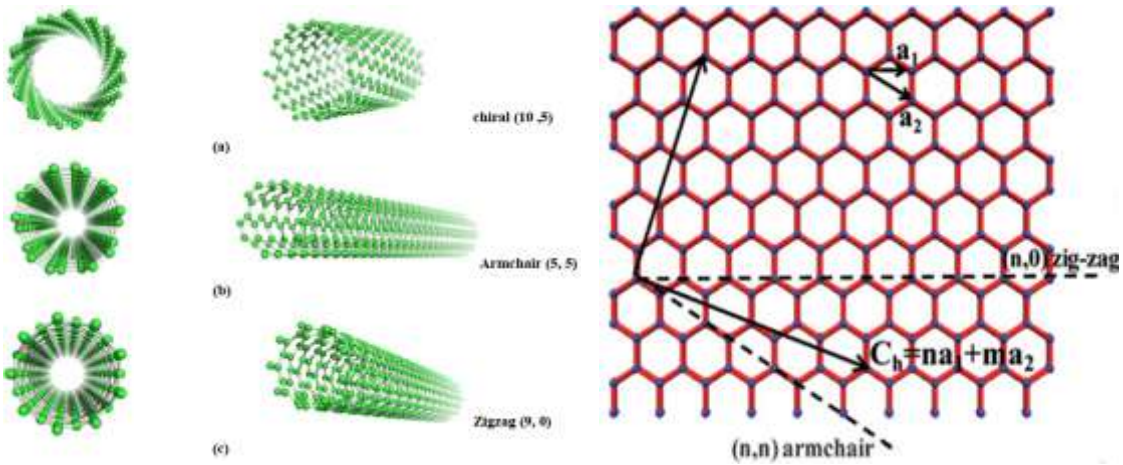


Figure I.12. *Structure of a carbon nanotube with fullerenes [109].*

- Tubes are referred to as "armchair" when the helicity angle θ equals 30°, which corresponds to equal chirality indices (n, n).
- Tubes are referred to as "zigzag" when the helicity angle θ is zero and one of the chirality indices is zero, specifically (n, 0).
- The third type, known as chiral nanotubes with indices (m, n), is characterized by an intermediate angle (0° < θ < 30°). These nanotubes exhibit a distinctive helical morphology and possess mirror symmetry due to their specific atomic arrangement.

Figure I.13 depicts the three main structural types of carbon nanotubes, while **Figure I.14** presents single-walled carbon nanotubes synthesized on a planar sapphire substrate using the chemical vapor deposition (CVD) technique, showcasing their aligned morphology:



(a) *(b)*

Figure I.13. ***(a)*** *Nanotubes with different structural types: (a) chiral nanotube characterized by the indices (10, 5), (b) armchair nanotube with indices (5, 5), and (c) zigzag nanotube represented by (9, 0) (simulation based on [110]).* ***(b)*** *Structure of a two-dimensional graphene plane with hexagonal lattice as described using the two base vectors* $\overrightarrow{a_{1_1}}$ *and* $\overrightarrow{a_2}$*[111].*

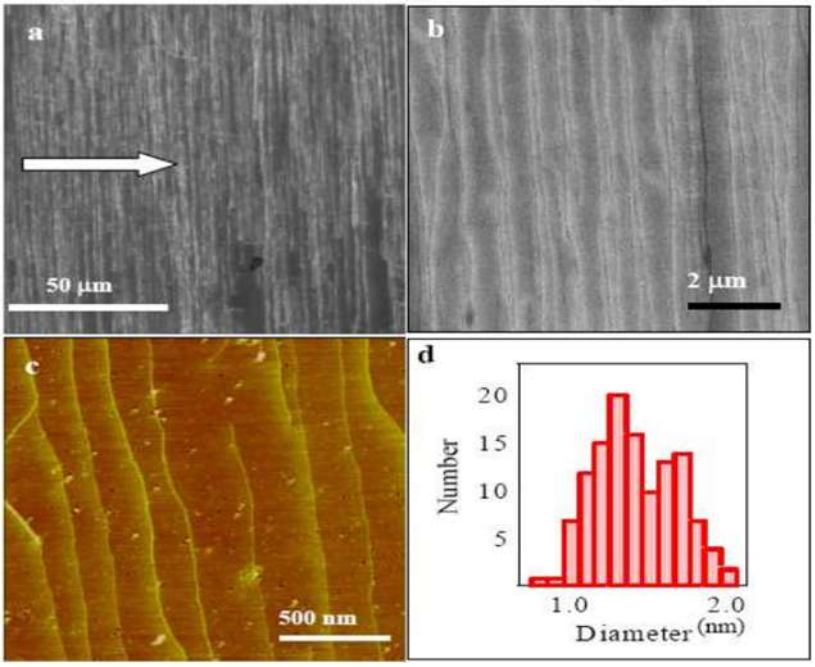


Figure I.14. *Single-walled carbon nanotubes (SWCNTs) on a plane sapphire substrate synthesized by (CVD) technique. (SEM) images at low magnification (a) and high magnification (b), (c) atomic force microscopy (AFM) image of aligned SWCNTs; (d) the diameter distribution of the synthesized SWCNTs [112,113].*

b) Multi-walled Carbon Nanotubes (MWNTs)

Multi-walled carbon nanotubes (MWNTs) consist of several concentric cylindrical graphene layers, each with distinct chirality, together forming a turbostratic structure [3,54]. This turbostratic arrangement is similar to that found in turbostratic graphite, which is characterized by the irregular stacking of graphene sheets [107]. The spacing between adjacent layers in MWNTs is approximately 3.4 Å, closely corresponding to the interlayer distance in natural graphite [3], MWNT diameters vary depending on the number of graphene layers, typically ranging between 2 and 25 nanometers, with lengths extending from 20 to 80 micrometers [54,114]. **Figure I.15** presents a graphical depiction of a multi-walled carbon nanotube (MWNT) on the left alongside its corresponding transmission electron microscopy (TEM) image on the right, providing a clear visualization of its multilayered cylindrical structure.

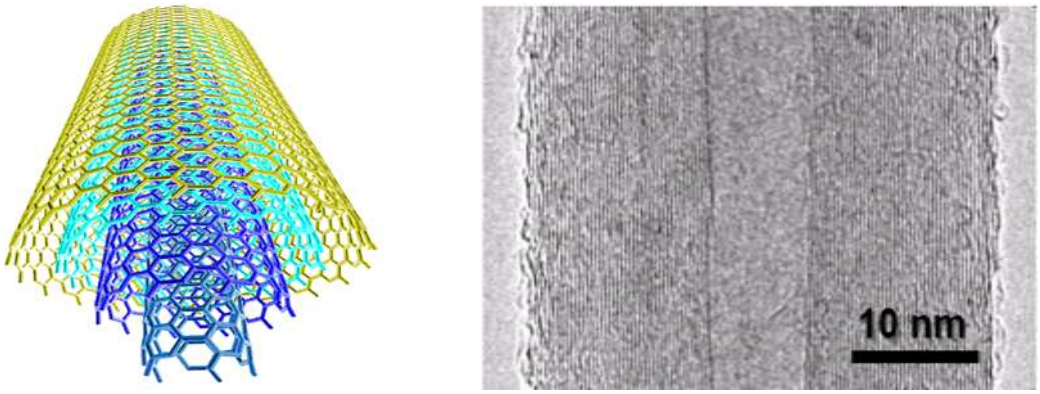


Figure I.15. *A Multi-Walled Nanotube (MWNT) graphically depicted on the left, and its image obtained by transmission electron microscopy (TEM) on the right [115].*

I.2.2 Synthesis Methods of Carbon Nanotubes

Currently, several synthesis techniques are employed to produce carbon nanotubes (CNTs), including electric arc discharge, laser ablation, and chemical vapor deposition (CVD). These approaches facilitate the mass production of both multi-walled carbon nanotubes (MWNTs) and single-walled carbon nanotubes (SWNTs), with the capability to tailor nanotube diameters. While some methods have reached commercialization, ongoing research aims to enhance production efficiency and yield optimization.

I.2.2.1 Arc Discharge

The synthesis method for single-walled carbon nanotubes by electric arc discharge was first described by Iijima et al. and Bethune et al. This method is schematically illustrated in **Figure I.16**. In this approach, Carbon electrodes with diameters of approximately 5–20 mm are separated by a distance of about 1 mm. A voltage of 20–25 V and a direct current ranging from 50 to 120 A are applied between these electrodes [116]. The experiment is typically conducted under a helium atmosphere at a pressure of approximately 500 torr with a flow rate of about 5–15 $mL \cdot s^{-1}$. When the electric arc is initiated, a carbon deposit forms around the cathode. It is within this deposit that carbon nanotubes are found. In general, the electric arc synthesis method produces nanotubes with diameters ≤ 1.5 nm [99]. Similar to the laser ablation technique, the use of catalysts is necessary to obtain single-walled carbon nanotubes. The same types of catalysts are employed in both methods. The raw product also contains amorphous carbon, fullerene species (in small quantities), and catalyst residues. Therefore, as with the laser ablation method, purification of the raw product is essential to isolate a sample containing exclusively nanotubes, a process that unfortunately adversely affects the quality of the nanotubes. Finally, similarly to the laser ablation method, the electric arc technique allows for the production of relatively large quantities of single-walled carbon nanotubes, on the order of grams per day [117].

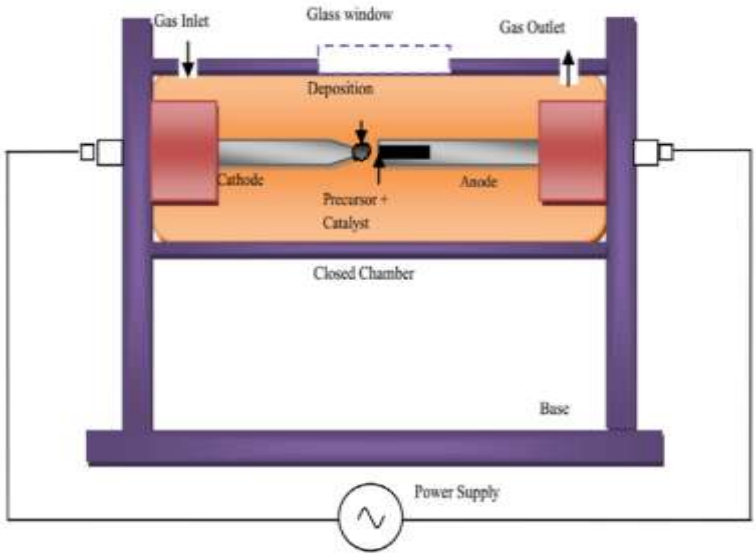


***Figure I.16**. Schematic diagram illustrating the fundamental principle of the electric arc synthesis method [118].*

I.2.2.2 Laser Ablation

Another effective technique for the synthesis of single-walled carbon nanotubes is laser ablation. Historically, laser ablation was the first method employed to generate fullerenes in the gas phase. In this process, carbon sublimation is induced by a pulsed laser beam focused onto the surface of a graphite disk under an inert gas flow. The graphite target is positioned at the center of a furnace, which is maintained at a temperature of approximately 1200°C. The sublimated carbon vapors are transported to a collector where they condense it is illustrated in **Figure I. 17** [119-121].

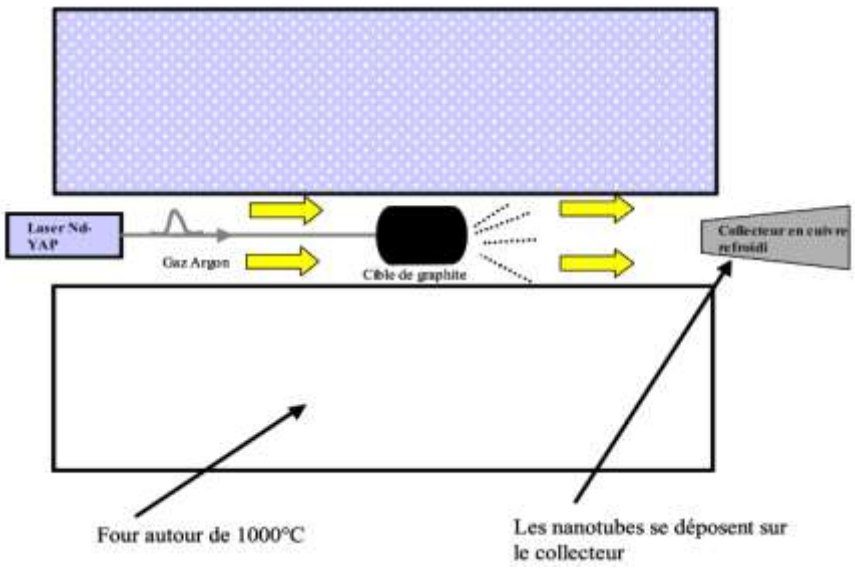


Figure I.17. *Schematic illustration of the principle of the laser ablation method [122].*

I.2.2.3 Catalytic Growth of Carbon Nanotubes in the Gas Phase via the HiPco Process

The catalytic gas-phase growth method for synthesizing carbon nanotubes, known as HiPco (High Pressure Carbon Monoxide), was developed in 1998 by the research group led by R.E. Smalley at Rice University. This technique involves introducing a gaseous flow of carbon monoxide along with a catalytic precursor into a high-pressure reactor maintained at 30–50 atmospheres and elevated temperatures ranging between 900 and 1100°C [123,124]. Under these conditions, the catalyst precursor decomposes, generating iron nanoparticles that serve as active catalytic sites [123]. Subsequently, carbon monoxide molecules react at the catalyst surface, producing carbon dioxide and depositing atomic carbon. Consistent with chemical vapor deposition (CVD) mechanisms, these carbon atoms migrate along the edges of the

catalyst nanoparticles, assembling into single-walled carbon nanotubes (SWNTs). By precisely controlling the synthesis parameters, the process can achieve nearly 100% selectivity in producing SWNTs, with nanotube diameters controllable down to approximately 0.7 nm. Further advancements by Smalley's startup, Carbon Nanotechnologies Inc., have enabled the scalable production of high-purity SWNTs [124], facilitating their application in various industrial sectors including electronics, biomedicine, and energy [125]. **Figure I.18** illustrates the chemical vapor deposition (CVD) process.

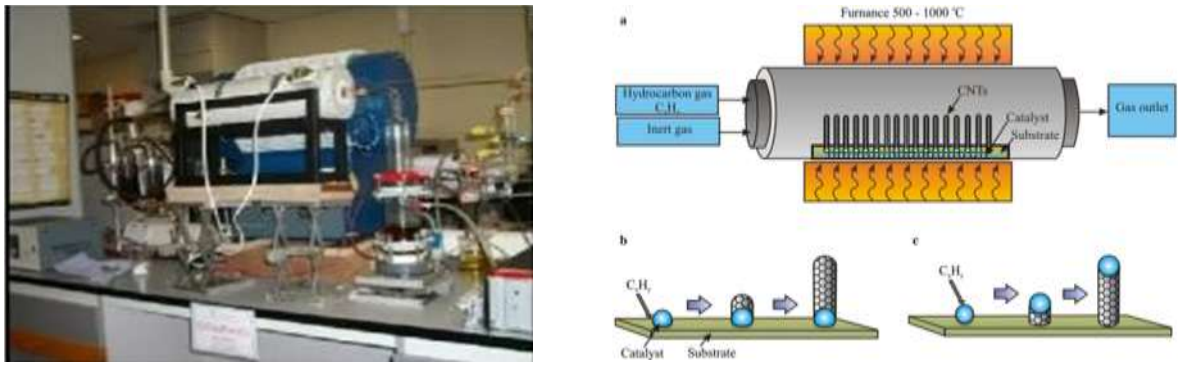


Figure I.18. *Chemical vapor deposition (CVD) process. (a) Basic schematic of a CVD reactor for the synthesis of carbon nanotubes (CNTs), (b) model illustrating the base-growth mechanism of CNT development, (c) model illustrating the tip-growth mechanism of CNT development [126,127].*

Techniques like density gradient ultracentrifugation enable separation of semiconducting and metallic CNTs, critical for transistor arrays [128]. Recent progress in catalyst engineering and growth conditions aims to achieve chirality-specific growth for device uniformity [129]. Several techniques exist for the synthesis of carbon nanotubes (CNTs), each with unique advantages and limitations. **Table I.2** provides an overview of the most common synthesis methods, including chemical vapor deposition (CVD), laser ablation, and arc discharge. These methods vary in their operational conditions, catalysts, carbon sources, yields, and control over nanotube quality and morphology, guiding the selection of appropriate synthesis procedures for specific applications.

Table I.2: Common synthesis techniques for carbon nanotubes (CNTs).

Method	Yield	Description
Laser ablation	**< 75**	A high-power laser beam is focused onto a carbon-containing gas (such as methane or carbon monoxide), inducing laser ablation that generates a small quantity of clean carbon nanotubes. This synthesis method typically produces long nanotubes with diameters ranging from approximately 1.0 to 2.0 nm.
Arc discharge	**< 75**	An electric arc formed between two carbon electrodes, with or without the presence of a catalyst, generates a carbon vapor from which nanotubes spontaneously self-assemble. This technique typically yields a large amount of material containing impurities. The resulting carbon nanotubes are generally short in length, with diameters ranging from approximately 0.6 to 1.4 nm.
CVD	**> 75**	Chemical vapor deposition (CVD) is a widely used technique for synthesizing multi-walled carbon nanotubes (MWCNTs) and single-walled carbon nanotubes (SWCNTs), typically yielding nanotubes of relatively lower structural quality. The SWCNTs produced by CVD exhibit a broad diameter distribution, which can be challenging to control precisely. However, this method is relatively simple to implement and scale up, facilitating commercial production. The carbon nanotubes obtained are generally long, with diameters varying approximately between 0.4 and 4 nm.

I.2.3 Properties of Carbon Nanotubes

Since their discovery, carbon nanotubes have demonstrated remarkable physical properties that have spurred extensive scientific research. Consequently, a wide range of potential applications has already been proposed and explored.

I.2.3.1 Chemical Properties

Carbon nanotubes (CNTs) exhibit a wide range of chemical properties, as outlined in [130]: One key feature is molecular grafting, a method used to alter the surface characteristics of nanotubes to separate them based on their electronic properties. Additionally, it is possible to modify the electronic behavior of semiconductor nanotubes by introducing atoms or molecules either inside single-walled carbon nanotube (SWCNT) bundles (known as intra-tubular intercalation) or between layers in multi-walled nanotubes (inter-planar intercalation). CNTs also have a large surface area, making them highly suitable for adsorption applications. Typically, single-walled carbon nanotubes have a specific surface area of less than 1,300 m^2/g, while multi-walled nanotubes can reach up to 2,700 m^2/g. Another notable attribute of carbon nanotubes is their strong chemical resistance and exceptional stability at high temperatures when in an inert atmosphere. Because of their insoluble nature, they cannot be dissolved in either organic solvents or water.

I.2.3.2 Electronic Properties

The remarkable electronic properties of single-walled carbon nanotubes (SWCNTs) enable their use in fabricating devices and components such as metallic interconnects and vias [131], as well as diodes [132] and transistors, depending on whether they exhibit metallic or semiconducting behavior. The electronic nature of a SWCNT is determined by its chirality, which dictates whether it behaves as a semiconductor or a metal. As illustrated by the graphene band structure diagram shown in **Figure I.19** [133], **Figure I.19** illustrates the energy band diagrams of a graphene sheet in two scenarios: (a) the metallic case where the conduction and valence bands intersect, and (b) the semiconducting case where an energy bandgap exists ,within the Brillouin zone, the conduction band (π^*) and the valence band (π) converge at the K points, forming valleys. At the K point, the energy difference between these two bands defines the bandgap of the nanotube. From a cross-sectional perspective, if the conduction and valence bands intersect or the bandgap is less than a few tens of meV, the nanotube exhibits metallic properties; otherwise, it behaves as a semiconductor. For semiconducting nanotubes, the Fermi level lies at the midpoint of the bandgap.

The electronic properties of carbon nanotubes depend on their chirality indices (n, m) according to the following rules:

- *When n = m, the nanotube behaves as a metal.*
- *When n – m = 3i (where i is an integer), the nanotube exhibits a small bandgap and is generally considered metallic.*
- *When n – m ≠ 3i, the nanotube displays semiconducting behavior.*

The density of states (DOS) of the carbon nanotube is directly derived from its dispersion relation, as shown in **Figure I.20,** for a nanotube with chirality (19, 0). In this figure, the valence and conduction bands are separated by a direct band gap (Eg ≈ 0.55 eV). The Van Hovesingularities are also visible at each subband confirming the quasi-one-dimensional nature of the carbon nanotube [97].

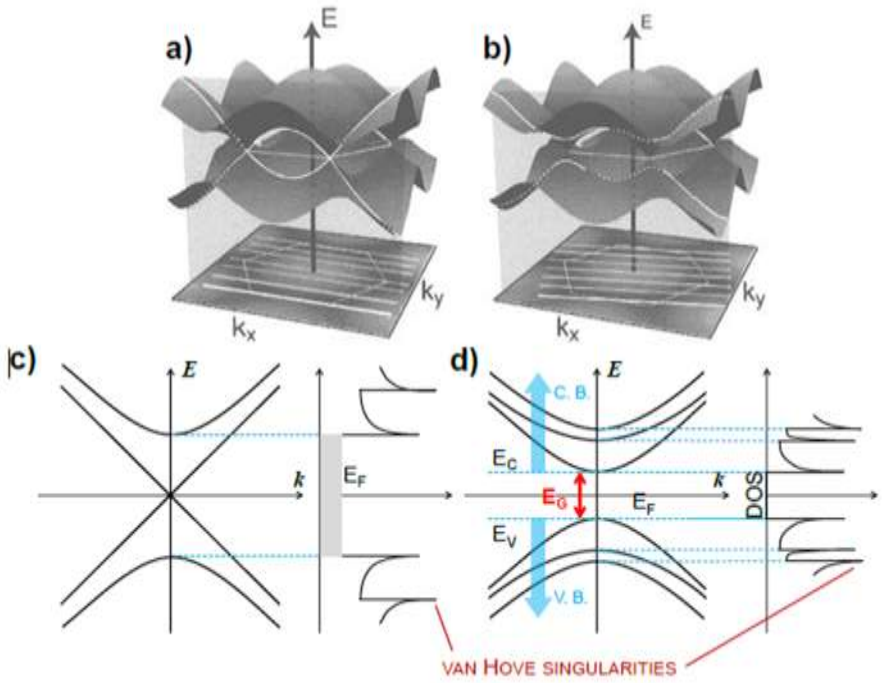
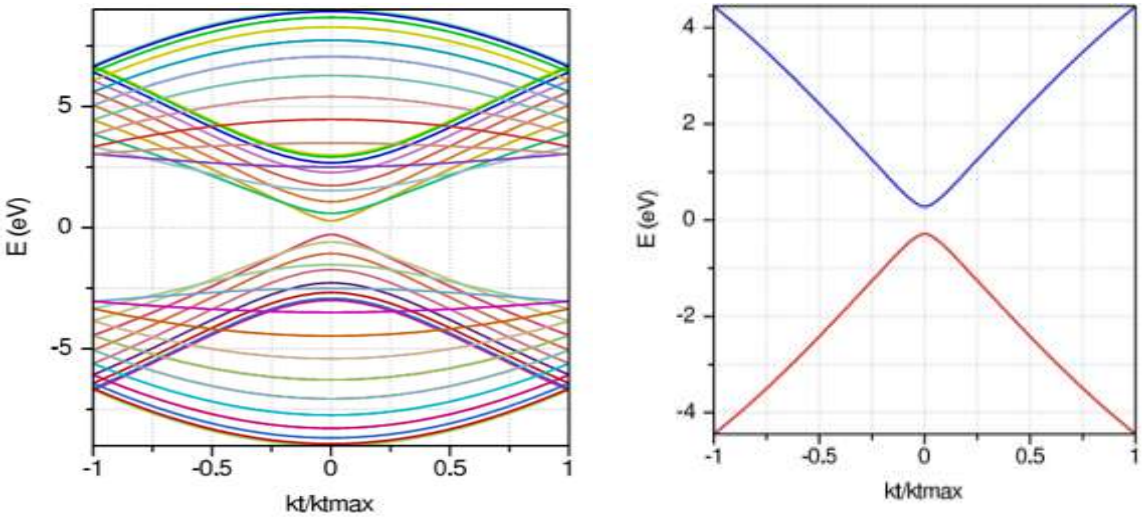


Figure I.19. *Energy band diagram of a graphene sheet, a) metallic case, b) semiconducting case [133].*



(a) **(b)**

Figure I.20*. (a) Energy band profile of a semiconducting carbon nanotube with chirality (19, 0), obtained from tight-binding method calculations. (b) Illustration of the first subband [97].*

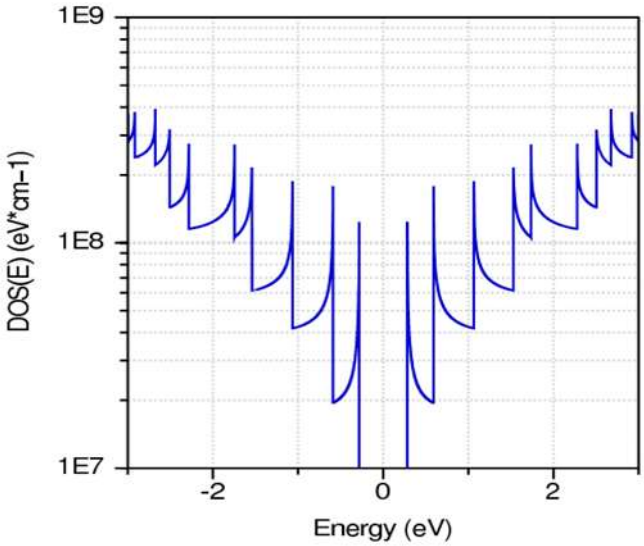


***Figure I.21**. Density of states of a semiconducting carbon nanotube with chirality (19,0). The peaks correspond to the Van Hove singularities of the different subbands [97].*

I.2.3.3 Optoelectronic Properties

Semiconducting carbon nanotubes possess a direct bandgap, a characteristic that is advantageous for optoelectronic device applications. For light emission purposes, the use of ambipolar nanotube transistors is particularly beneficial, as they enable simultaneous conduction of both holes and electrons. For sufficiently long channels (i.e., the distance charge carriers must travel) where the interaction rate is significant, the recombination current reaches its maximum value [134]. The light emission originates from a specific location within the channel, which can be altered by adjusting one of the applied voltages. Hole and electron currents reside in the valence and conduction bands, respectively. Carbon nanotubes exhibit both photoluminescence and photoconductivity: upon photon absorption, an exciton is generated that can either re-emit a photon (photoluminescence) or, under an applied bias, generate and separate electron-hole pairs contributing to photoconduction [134].

Vertical carbon nanotubes serve as electron emitters in field emission applications, where electrons are released from the nanotube apex. An electrically biased mesh placed above the nanotubes designed with openings to permit electron flow establishes the electric field required for emission. Utilizing this configuration, arrays of field emission devices can be developed, enabling technologies such as microwave amplifiers and electron beam sources [106].

I.2.3.4 Mechanical Properties

Carbon nanotubes exhibit exceptional stiffness, comparable to that of steel, while maintaining an extremely low density. Their key mechanical characteristics include the following attributes [135]:

Hardness: The mechanical strength of carbon nanotubes is theoretically expected to be approximately 200 times greater than that of steel, while being six times lighter for an equivalent cross-sectional area. This outstanding performance is primarily attributed to their hexagonal lattice geometry, which enables a uniform distribution of stress and strain. Moreover, these mechanical properties vary depending on the type of nanotube: multi-walled carbon nanotubes (MWCNTs) exhibit significantly higher strength compared to single-walled carbon nanotubes (SWCNTs) [99].

Elasticity: Elasticity refers to the mechanical stress necessary to produce a 100% elongation of a material's original length (i.e., doubling its length). Carbon nanotubes undergo permanent deformation or fracture well before reaching this strain level [134]. Nevertheless, carbon nanotubes exhibit remarkable elasticity and flexibility, enabling them to sustain significant mechanical deformation without damage [135]

I.2.3.5 Thermal Properties

Carbon nanotubes exhibit highly anisotropic thermal conductivity, with values ranging from approximately 1800 to 6600 $W \cdot m^{-1} \cdot K^{-1}$. This performance makes them excellent thermal conductors about five times more conductive than copper and nearly thirty times more than iron (see the following table). Due to these characteristics, carbon nanotubes are considered promising materials for efficient heat dissipation in electronic devices and circuits, **Tables I.3** and **I.4** provide comparative data on the thermal conductivity of carbon nanotubes (CNTs) relative to other materials, highlighting their exceptional performance as heat conductors.

I.2.3.6 Capillarity Properties

Carbon nanotubes (CNTs) can be viewed as hollow "nanowires" that can be filled through capillary action. This enables the encapsulation of metals inside the nanotubes (see **Figure I.22(a)**) as well as macromolecules such as fullerenes (**Figure I.22(b)**). Fullerene-based structures called "peapods" were first reported by Smith et al. Metallofullerenes, which are fullerenes containing one or more metal atoms trapped inside their carbon cage structure, can

also be encapsulated within single-walled carbon nanotubes (SWNTs) (**Figure I.22(b)**). Various metals, mainly rare earth elements, can be isolated inside SWNTs either as individual atoms or atomic chains. This rare structure allows individual atoms to be directly observed and analyzed.

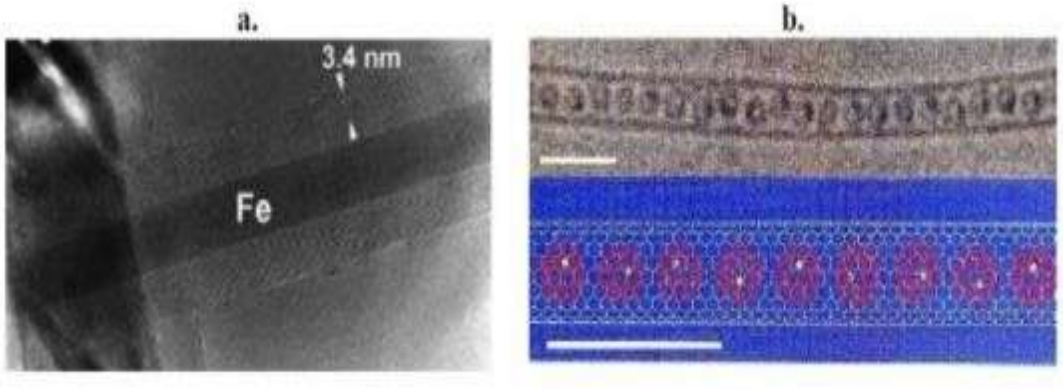


Figure I.22. ***(a)*** *Iron encapsulated in a multi-walled nanotube [150],* ***(b)*** *C82 encapsulated in a single-walled nanotube [151].*

Table I.3. *Comparison of the thermal conductivity of CNTs with that of other materials [136].*

	Thermal conductivity (W /m .k)	Scale
MWCNT	1800-3000	Nanometric
SWCNT	2500-6600	Nanometric
Iron	80	Massive
Gold	317	Massive
Copper	485	Massive
Diamond	1000	Massive

Table I.4. *Reported Thermal Conductivity of Carbon Nanotubes [137].*

Classified	Researcher	Year	Method	Chirality	Temp. [K]	Thermal Conductivity [W $m^{-1}K^{-1}$]
Low thermal	Moreland et al.[138]	2004	MD, Brenner potential	(10,10)	300	215–831
Conductivity	Maruyama[139]	2003	MD, Tersoff-Brenner bond order potential	(5,5),(8,8), (10,10)	300	260–400 for (10,10)
Medium thermal conductivity	Osman and Srivastava[140]	2001	MD, Tersoff-Brenner potential	(5,5), (10,10), (15,5)	300	1700 for (10,10)
	Grujicic et al.[141]	2004	MD, Adaptive Intermolecular Reactive Empirical Bond Order (AIREBO) potential	(10,10) (18,0) (14,6)	300	1780 for (10,10)
	Lindsay et al.[142]	2010	Boltzmann transport equation	-	300	2500
	Che et al.[143]	2000	MD, equilibrium Green-Kubo method based on the Brenner potential	(10,10)	300	2980
	Zhang et al.[144]	2004	MD, non-equilibrium Green–Kubo method used on the Brenner potential	(11,11) (20,0) (10,13)	300	3700 for (11,11)
High thermal conductivity	Ren et al.[145]	2010	Non-equilibrium MD method	(10,10)	300	6000
	Berber et al.[146]	2000	MD	(10,10)	300	6600
	Donadio and Galli[147]	2007	MD and Boltzmann transport equation	10,0)	300	7000
	Mir et al.[148]	2012	CM, Solid continuum elements	(10,10)	300	9750
	Yao et al.[149]	2005	MD	(10,10)	300	1-4. 10^5

I.2.4 Field Emission of Carbon Nanotubes

Carbon nanotubes have recently proven to be excellent systems for field emission. Their low electric field threshold for emission and high emission current density make them attractive for technological applications [152].

I.2.4.1 Aspect Ratio

One notable property of carbon nanotubes (CNTs) is their high aspect ratio, which means that a lower amount of CNT is needed compared to other conductive additives to achieve similar electrical conductivity. This high aspect ratio gives CNTs unique electrical conductivity characteristics compared to traditional additives such as chopped carbon fiber, carbon black, or stainless-steel fiber.

I.2.4.2 Absorption

Carbon nanotubes and CNT composites have become effective absorbing materials due to their light weight, increased flexibility, high mechanical strength, and superior electrical properties. Consequently, CNTs are considered ideal candidates for air and water gas filtration.

The absorption frequency range for single-walled carbon nanotube (SWNT)-polyurethane composites extends from 6.4 to 8.2 GHz (band width 1.8 GHz), 7.5 to 10.1 GHz (2.6 GHz band width), and 12.0 to 15.1 GHz (3.1 GHz band width) [153]. Significant research has already been conducted to replace activated carbon with CNTs in certain ultra-pure applications.

I.2.5 Applications of Carbon Nanotubes

The unique electronic and optoelectronic properties of carbon nanotubes form the foundation for a wide range of applications. CNTs exhibit remarkable qualities as structural materials, with potential uses including:

Textiles: CNTs can be used to produce fabrics that are waterproof and tear-resistant.

Body Armor: CNT fibers are employed in combat vests, which monitor the wearer's condition and provide ballistic protection.

Concrete: Incorporating CNTs in concrete enhances its tensile strength and prevents crack propagation.

Polyethylene: CNT fibers can be blended with polyethylene, increasing the polymer's elastic modulus by up to 30%. Sports Equipment: CNTs improve the strength and lightness of golf balls, golf clubs, tennis rackets, bicycle components, and baseball bats.

Bridges: CNTs have the potential to replace steel in suspension bridges and other structural elements.

Flywheels: Due to their high strength-to-weight ratio, CNTs enable flywheels to achieve very high rotational speeds.

Fire Protection: Thin layers of papier-mâché reinforced with dense, compact CNT or carbon fiber paper can effectively reflect heat and protect objects from fire.

I.2.5.1 Chemistry Field

Carbon nanotubes (CNTs) have significant applications in the field of chemistry, including the following:

Pollution Filters: CNTs are among the top materials used for pollution filters due to their large surface area and high absorption capacity. The conductivity of CNTs changes when they come

into contact with polluted gases, enabling the detection and filtration of contaminated air. CNT membranes effectively filter carbon dioxide from power plant emissions.

Water Filtration: CNT-based membranes facilitate water purification by allowing small particles like water molecules to pass through while blocking larger ones such as chloride ions. This filtration method can reduce distillation costs by up to 75%.

Chemical Nanowires: CNTs are utilized to create nanowires from materials like gold, zinc oxide, and gallium arsenide. Gold-based CNT nanowires exhibit high selectivity and sensitivity for detecting hydrogen sulfide (H_2S). Zinc oxide (ZnO) CNT nanowires are useful in light-emitting devices and vibrational energy harvesters.

Sensors: CNT-based sensors are capable of detecting various parameters including temperature, atmospheric pressure, chemical gases such as carbon monoxide and ammonia, molecular pressure, and mechanical stress. These sensors operate primarily through the generation of electrical current or voltage, which is influenced by the adsorption of target molecules on the CNT surface. An example of a CNT-based gas detection device is shown in **Figure I.23**.

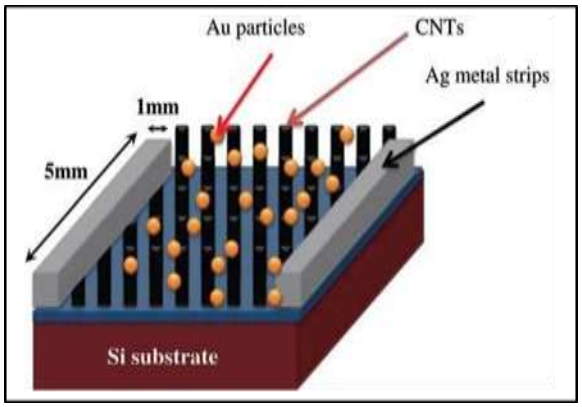


Figure I.23. *Fabricated gas detector [154].*

I.2.5.2 Mechanical Engineering Field

Carbon nanotubes (CNTs) also have promising applications in various mechanical engineering areas, including:

Oscillators: CNT-based oscillators have achieved performance speeds exceeding those of other technologies, surpassing 50 GHz. Researchers have demonstrated molecular oscillators capable of operating at frequencies reaching several gigahertz. These oscillators primarily rely on the

low-friction and wear-resistant bearing properties of multi-walled CNTs, which have diameters ranging from about 1 nanometer to several tens of nanometers.

Waterproofing: CNTs can be employed to create superhydrophobic cotton fabrics through coating and dipping processes. This method uses UV-activated nitrene chemistry to chemically modify the cotton surface from hydrophilic to superhydrophobic, resulting in an apparent water contact angle of 154º. Since CNTs are covalently bonded to the cotton surface, the resulting super hydrophobicity exhibits excellent stability and long-lasting durability.

I.2.5.3 Electromagnetic Applications

Carbon nanotubes (CNTs) can be engineered to function as electrical conductors, semiconductors, or insulators. Their applications include:

Bucky Paper: These thin sheets of nanotubes are 250 times stronger and 10 times lighter than steel. They can be utilized as heat dissipation materials for particleboards, backlighting in LCD screens, or as Faraday cages to shield electronic devices in aircraft.

Light Bulb Filaments: CNTs present a viable alternative to tungsten filaments in incandescent lamps.

Magnets: Powerful magnetic fields can be generated using multi-walled CNTs coated with magnetite.

Solar Cells: Germanium-CNT diodes exploit the photovoltaic effect. In certain solar cells, nanotubes replace indium tin oxide (ITO), allowing light to penetrate active layers and generate photocurrent.

Electromagnetic Antennas: Due to their durability, lightness, and conductive properties, CNTs serve effectively as antennas for radio and other electromagnetic devices. The skin effect in CNTs is minimal at high frequencies because of the additional kinetic inductance, resulting in low power dissipation and thus high antenna efficiency.

I.2.5.4 Optical Domain

Carbon nanotubes (CNTs) are grown densely, resembling a field of grass where each nanotube stands apart like an individual blade. This arrangement causes light particles to bounce between the nanotubes, resulting in complete absorption and conversion of the light into heat.

Consequently, CNTs exhibit extremely high absorbance across a broad spectrum, ranging from the far ultraviolet (FUV, 100–200 nm) to the far infrared (FIR, 50–1000 μm).

I.2.5.5. Electrical Circuits

CNTs are attractive materials in both fundamental science and technology, demonstrating unique electrical properties suitable for electronic devices such as carbon nanotube field-effect transistors (CNTFETs) and CNT diodes. By chemical doping and polymer coating, CNTs can form p–n junction diodes, which may be utilized in computer chips. Due to their exceptional thermal conductivity, CNT diodes have the potential to aid in dissipating heat from computer chips.

I.2.5.6. Interconnections

Thanks to their electrical conductivity, metallic single walled carbon nanotubes (SWNTs) are effectively used as interconnections between metal layers in integrated circuit (IC) fabrication. CNTs offer better electrical and thermal conductivity compared to copper and being non-bulk metals, they exhibit minimal skin effects, which hampers high-frequency transmission in copper. Due to their higher current capacity (up to 1000 MA/cm² for a single CNT), CNT interconnections address reliability issues currently affecting copper at the nanoscale, potentially offering significant advantages over copper in terms of crosstalk, delay, and power dissipation.

I.2.5.7. Transistors

Carbon nanotubes (CNTs) can serve as conductive channels in transistor configurations, as illustrated in **Figure I.24**. Two transistor architectures have been developed: in both, CNTs connect the source and drain electrodes and exhibit excellent performance in applications such as memory design, amplifiers, sensors, and detectors. In one device architecture, a single nanotube links the source and drain. In the other, a random network of nanotubes forms the conductive channel. The advantages of CNTFETs over traditional silicon MOSFETs (Si-MOSFETs) include: CNTFETs deliver a higher drive current than Si-MOSFETs. CNTFETs exhibit a transconductance approximately four times greater than that of Si-MOSFETs. The average carrier velocity in CNTFETs is nearly twice that in Si-MOSFETs.

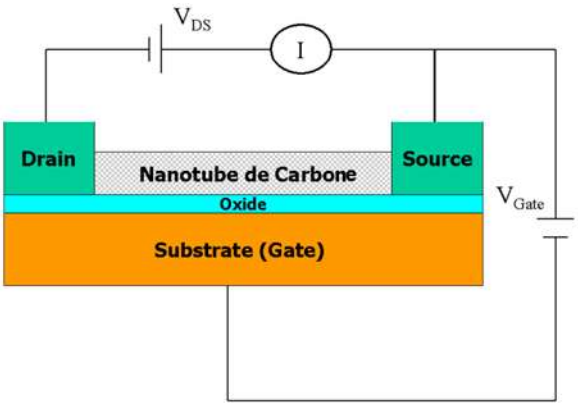


***Figure.I.24**. Diagram of a transistor using a carbon nanotube as the channel [155].*

I.3. Toxicity of Carbon Nanotubes

Due to their extremely small size, carbon nanotubes (CNTs) can pose health risks. Studies have shown that exposure to very high concentrations of CNTs may lead to lung inflammation [156]. The toxicity of nanoparticles like CNTs varies depending on factors such as their size, number of walls, and how they are manufactured. Researchers have found it challenging to thoroughly investigate these toxicological effects because of their complexity. A key concern is that nanoparticles have a large surface area, which increases their chemical reactivity and potential toxicity. Cellular toxicity effects have also been noted when these nanoparticles are introduced into biological systems [157]. It remains difficult to definitively assess the health risks of CNTs, as many variables influence the body's response to exposure. While some beneficial effects, including antibacterial properties, have been identified, the overall safety of CNTs is still uncertain.

I.4. Graphene Nanoribbons (GNRs)

Graphene nanoribbons (GNRs) are fundamental building blocks in the development of graphene-based nanoelectronics technology. These GNRs are narrow strips of graphene with widths typically ranging from a few nanometers to several tens of nanometers. The confinement of electrons in one dimension within these narrow structures leads to quantum mechanical effects that significantly alter their electronic properties compared to infinite graphene sheet. This quantum confinement effect is responsible for the opening of a bandgap in GNRs, a crucial feature for their application in semiconductor devices, as pristine graphene is a zero-bandgap material [158]. The ability to engineer this bandgap by controlling the GNR's width and edge configuration is a key advantage that positions GNRs as a compelling alternative to traditional silicon-based semiconductors.

Figure I.25 demonstrates representative top-down fabrication techniques for graphene nanoribbons (GNRs). Panel (a) depicts a GNR produced via standard electron-beam lithography, while panel (b) shows chemically derived GNRs with widths below 10 nm, as revealed by atomic force microscopy (AFM). Panel (c) illustrates the fabrication process for lithographically patterned GNR arrays using aluminum lines as masks, and panel (d) presents AFM images of GNRs fabricated through anisotropic etching. These fabrication methods are critical because the structural characteristics of GNRs, especially their edge morphology, significantly influence their electronic and magnetic properties. Based on the carbon atom arrangements along their edges, GNRs are primarily classified into three types. The fabrication approaches outlined in **Figure I.25** are instrumental in controlling these structural features to tailor the functional properties of GNRs for various technological applications.

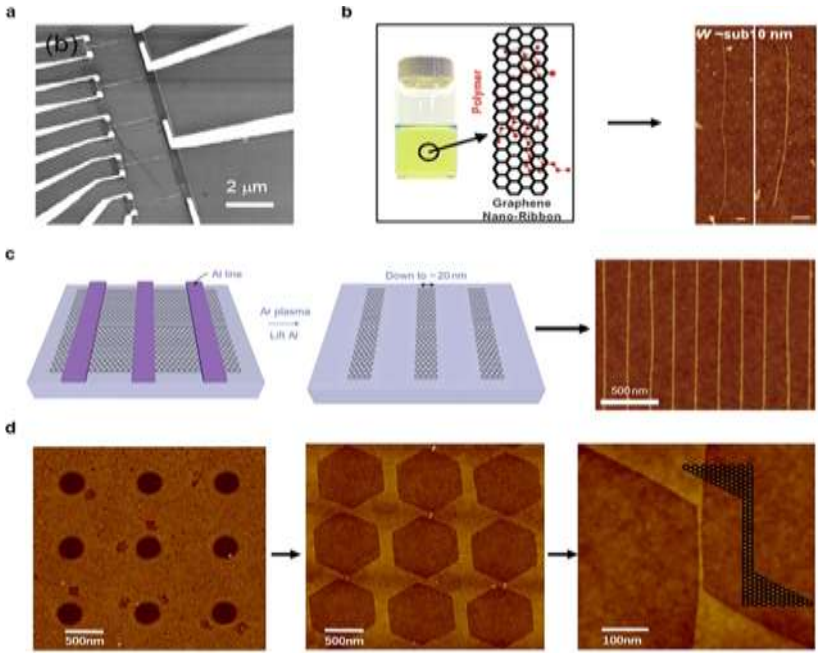


Figure I.25. *Representative top-down approaches for the fabrication of GNRs. a, GNR fabricated using standard E-beam lithography. b, Chemically derived GNRs. AFM image shows there are GNRs with a width of sub-10 nm. c, Schematics of the fabrication process of lithographically patterned GNR arrays with Al lines as masks. d, AFM images of fabricating GNRs using anisotropic etching. Panel (a) is adapted from [159]. An irregular sample of black, shiny glassy carbon showing fractures and layers, next to a 1 cm³ black graphite cube for scale Panel (b) is adapted from [160-162].*

I.4.1 Edge Types

Figure I.26 depicts the edge structures and corresponding electronic band characteristics of graphene nanoribbons (GNRs). Panel (a) illustrates the three fundamental edge types of GNRs: zigzag, armchair, and chiral configurations. Panel (b) shows the theoretical relationship

between the bandgap size and GNR width, highlighting the influence of dimensional constraints on electronic properties. Panels (c) and (d) present detailed electronic band structures for armchair and zigzag GNRs, respectively. Additionally, panels (e) and (f) demonstrate the effects of an externally applied transverse gate voltage on the electronic states and density of states in zigzag GNRs. These data collectively emphasize the critical role of edge morphology in shaping the electronic behavior of graphene nanoribbons.

I.4.1.1 Armchair GNRs (AGNRs): They are characterized by edges that resemble the arm of an armchair, with carbon atoms forming a series of hexagons along the edge. The bandgap of AGNRs is quantized and depends on their width, specifically on the number of dimer lines (N) across the ribbon [163]. Theoretical studies have shown that AGNRs can be metallic or semiconducting depending on N, following a periodicity of 3. Specifically, AGNRs with N = 3p-1 (where p is an integer) are metallic, while those with N = 3p and N = 3p-2 are semiconducting [164]. This unique property allows for precise bandgap engineering by controlling the ribbon width during synthesis, which is crucial for their application in electronic devices and sensors.

I.4.1.2 Zigzag GNRs (ZGNRs): Zigzag GNRs (ZGNRs) possess edges that resemble a zigzag pattern. Unlike AGNRs, ZGNRs are predicted to be metallic regardless of their width, due to the presence of localized edge states [165]. These edge states lead to flat bands at the Fermi level, resulting in a zero bandgap. However, the application of an external electric field or chemical functionalization can induce a bandgap in ZGNRs, making them semiconducting [166]. The magnetic properties associated with these edge states also open up possibilities for spintronic applications. For gas sensing, the metallic nature of pristine ZGNRs might limit their sensitivity, as a change in conductivity due to gas adsorption would be less pronounced compared to a semiconducting material. Therefore, functionalization or gating strategies are often employed to modulate their electronic properties for sensing purposes.

I.4.1.3 Chiral GNRs: These GNRs have edges that are a combination of armchair and zigzag configurations, resulting in a helical structure. Their properties are intermediate between AGNRs and ZGNRs and are highly dependent on their specific chiral angle [158].

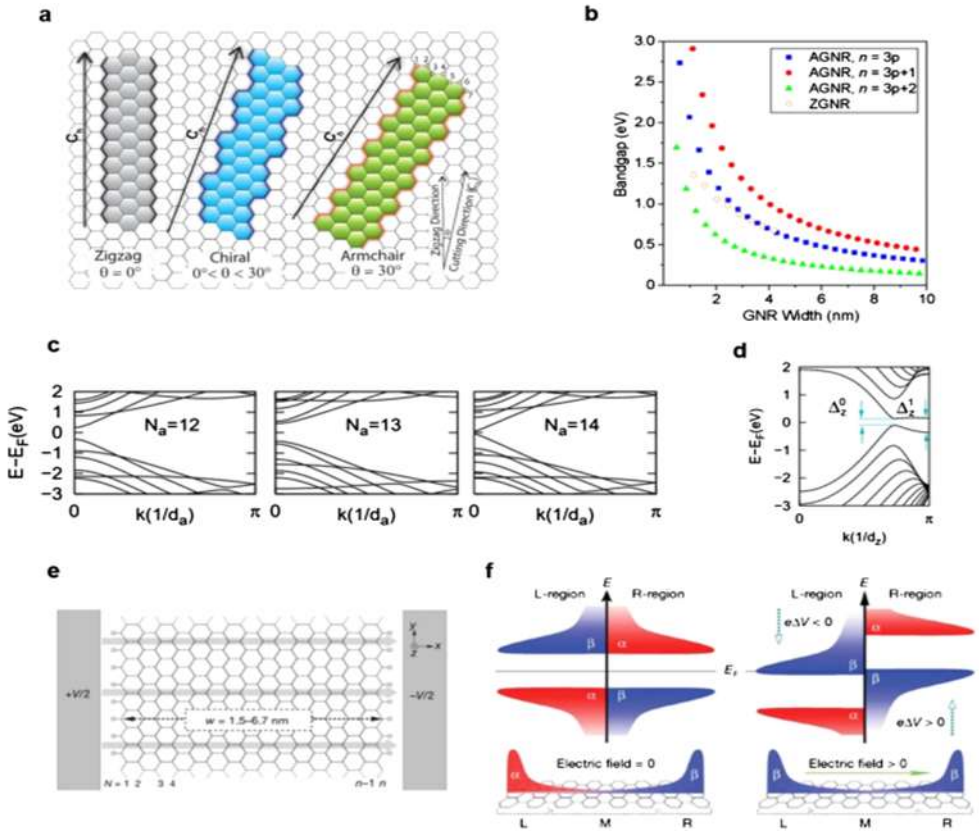


Figure I.26. *Edge structure and electronic band characteristics of graphene nanoribbons (GNRs). (a) Illustrations of the three fundamental GNR edge types: zigzag, armchair, and chiral configurations. (b) Theoretical correlation between the bandgap magnitude and the width of GNRs. (c) Electronic band structures for armchair GNRs with widths of N = 12, 13, and 14 carbon atom rows. (d) Band structure corresponding to a zigzag GNR of width N = 12. (e) Schematic depiction of a transverse gate voltage applied across a zigzag GNR. (f) Density of states of electronic states in a zigzag GNR, comparing conditions with and without an externally applied electric field. Panels (a) and (b) adapted from [167]; panels (c) and (d) from [168]; panels (e) and (f) from [169].*

I.4.2 Electronic Band Structure and Transport Properties

The extraordinary electronic properties of graphene and GNR stem from their unique atomic and crystallographic structures. Graphene's band structure is characterized by gapless, linear dispersions near the Fermi level forming conical Dirac points at the K and K′ valleys [170,171]. **Figure I.27** illustrates the electronic band structure of monolayer graphene, highlighting these characteristic features.

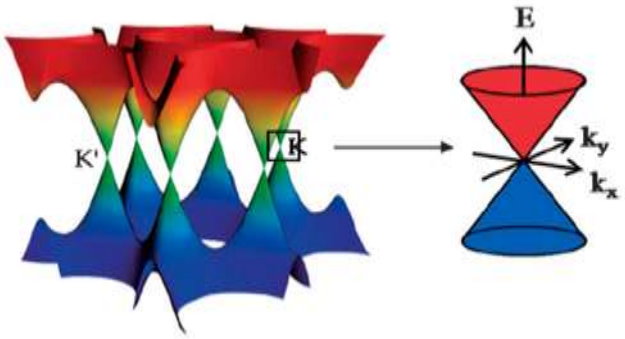


Figure I.27. *Electronic band structure of monolayer graphene. Adapted with permission from [172].*

The carriers behave as massless Dirac fermions with energies given by:

$$E = \hbar v_F |k| \qquad (I.4)$$

Where v_F is the Fermi velocity is (~10^6 m/s). This results in ultrahigh intrinsic carrier mobility exceeding 200,000 cm²/V·s in suspended graphene samples at low temperatures [173]. Although zero bandgap limits ideal transistor switching, graphene's ambipolar conduction allows carrier-type modulation with applied gate voltage [174,175]. Efforts focus on inducing a bandgap via quantum confinement (nanoribbons), substrate interactions, or chemical functionalization [176]. Ballistic transport over micron scales and minimal scattering contribute to graphene's suitability for high-frequency electronic and optoelectronic devices [177].

The most significant property of GNRs, especially for electronic applications, is their tunable bandgap. Unlike graphene, which is a zero-bandgap semimetal, GNRs can exhibit semiconducting behavior due to quantum confinement effects. The bandgap of GNRs can be precisely engineered by controlling their width, edge geometry, and by introducing defects or doping [158]. This tunability allows for the design of GNRs with specific electronic characteristics required for various device applications, such as field effect transistors (FETs), where a controllable on/off ratio is essential.

I.4.3 Synthesis Methods

I.4.3.1 Graphene

I.4.3.1.1 Mechanical Exfoliation (Scotch Tape Method)

The pioneering work by Geim and Novoselov in 2004 demonstrated the isolation of single-layer graphene through mechanical exfoliation of highly oriented pyrolytic graphite (HOPG) using adhesive tape [179]. **Figure I.28** presents a schematic representation of the mechanical exfoliation method, commonly known as the "Scotch tape" technique, for

synthesizing graphene This method, often referred to as the "Scotch tape method," involves repeatedly peeling layers from bulk graphite until single or few-layer graphene flakes are obtained. While simple and effective for producing high-quality, pristine graphene flakes suitable for fundamental research and proof-of-concept devices, mechanical exfoliation is inherently low-yield and not scalable for industrial applications. Nevertheless, it remains a crucial technique for studying the intrinsic properties of graphene due to the minimal introduction of defects or contaminants [95]. The "Scotch tape" method producing high-quality monolayers but limited in scale and yield [3].

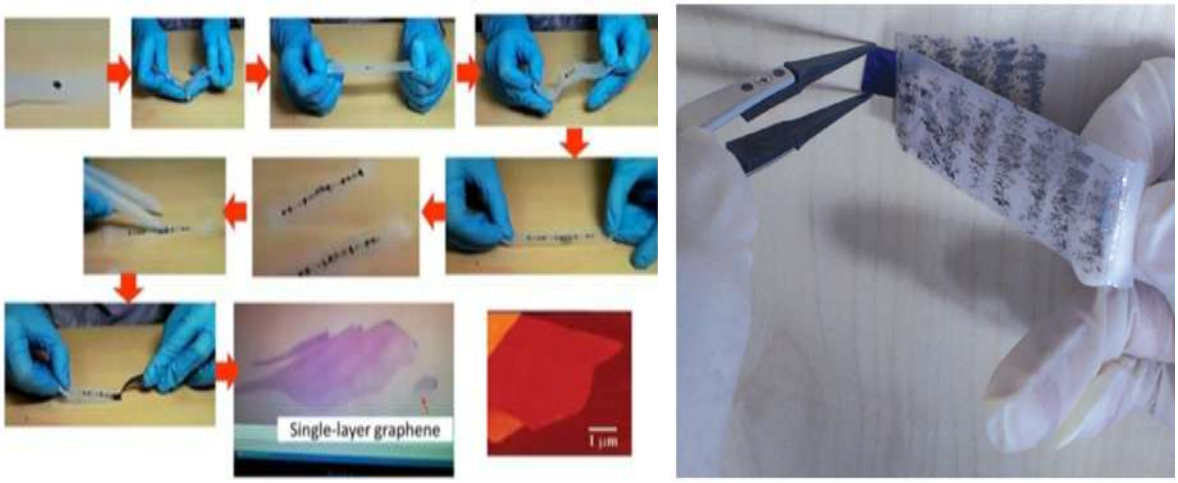


Figure I.28. *Schematic representation of the mechanical exfoliation (Scotch Tape) method for graphene synthesis [178].*

I.4.3.1.2 Chemical Vapor Deposition (CVD)

Chemical Vapor Deposition (CVD) has emerged as the most promising method for large-area, high-quality graphene synthesis, particularly for industrial applications [181]. **Figure I.29** depicts a schematic diagram of a conventional chemical vapor deposition (CVD) system, highlighting the key components and illustrating the flow of gases throughout the process. In CVD, a carbon-containing gas (e.g., methane, acetylene) is decomposed at high temperatures (typically 800-1100 °C) over a transition metal catalyst substrate, such as copper or nickel [182]. Carbon atoms dissolve into the metal and then precipitate out as graphene on the surface upon cooling. Copper is widely preferred due to its low carbon solubility, which facilitates the growth of single-layer graphene [182,183]. CVD-grown graphene offers excellent electrical properties and can be transferred to graphene [substrates, making it compatible with existing

semiconductor fabrication processes [184]. Challenges include controlling the number of layers, minimizing defects, and developing efficient and clean transfer techniques [182,184].

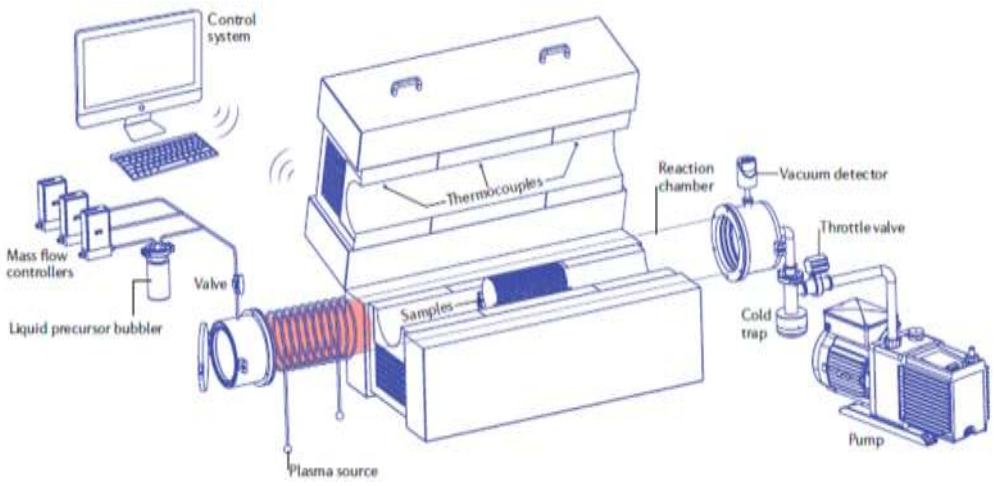


Figure I.29. *Schematic diagram of a standard chemical vapor deposition (CVD) apparatus. Reproduced with permission from Reference [180].*

I.4.3.1.3 Solution-Based Exfoliation

This method involves the exfoliation of graphite in liquid media to produce graphene flakes or graphene oxide (GO) [185]. Graphite can be exfoliated in organic solvents (e.g., N-methyl-2-pyrrolidone, NMP) or through chemical oxidation and subsequent reduction. The chemical oxidation of graphite yields graphene oxide, which is hydrophilic and can be readily dispersed in water. Subsequent reduction of graphene oxide (rGO) removes oxygen-containing functional groups, restoring some of graphene's electrical conductivity. While solution-based methods are highly scalable and cost-effective, the quality of the resulting graphene (especially rGO) is often lower than that obtained from mechanical exfoliation or CVD, with more defects and residual oxygen functionalities that can impact electronic properties [186].

I.4.3.1.4 Epitaxial Growth on SiC

Graphene can also be grown epitaxially on silicon carbide (SiC) substrates at high temperatures (typically >1200 °C) under vacuum or controlled atmosphere [187]. This method involves the thermal decomposition of SiC, where silicon atoms sublimate, leaving behind carbon atoms that reconstruct into graphene layers [188]. Epitaxial graphene on SiC offers the advantage of direct growth on a semiconducting substrate, eliminating the need for transfer processes and enabling the fabrication of robust devices [189]. The number of graphene layers

and their properties can be controlled by varying growth parameters. However, the high growth temperatures and the relatively high cost of SiC substrates are limiting factors for widespread adoption. **Figure I.30** illustrates the inherent trade-off between the quality of graphene produced and the associated economic costs. High-quality graphene synthesis often requires complex, resource-intensive methods that drive up production expenses, while more cost-effective approaches may compromise material quality. This balance between performance and cost remains a critical consideration in the scalable manufacturing of graphene for various applications.

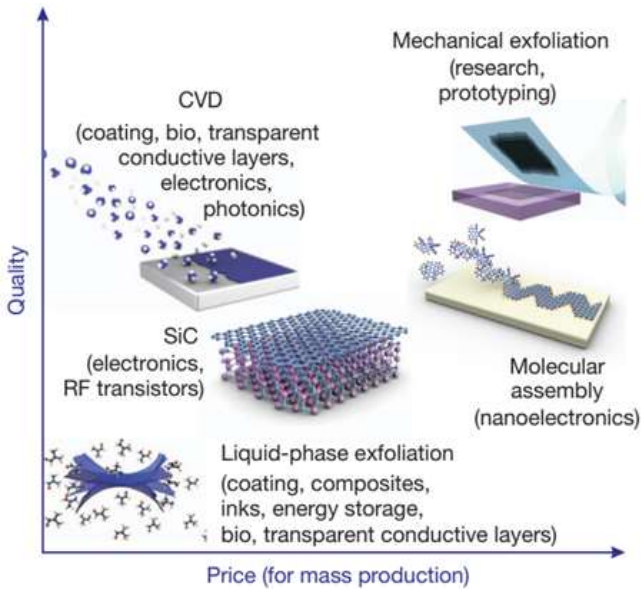


Figure I.30. *Illustration of the trade-off between graphene production quality and the associated economic costs. Adapted from [191]*

Each synthesis method presents a trade-off between material quality, scalability, and cost, dictating their suitability for different research and industrial applications. The choice of synthesis method is often critical for the performance of graphene-based devices, particularly in sensitive applications like gas sensing where material purity and structural integrity are paramount [190].

I.4.3.2. Synthesis Methods of GNRs

Various methods have been developed for the synthesis of GNRs, broadly categorized into top-down and bottom-up approaches [158].

I.4.3.2.1. Top-Down Approaches

Top-down methods involve cutting two-dimensional graphene into one-dimensional nanoribbons. These include

- ***Lithographic patterning***: GNRs can be fabricated by electron-beam lithography combined with oxygen plasma etching, typically yielding ribbons wider than 10 nm due to lithography resolution limitations [192].
- ***Chemical cutting***: This method can produce GNRs with widths below 10 nm. It involves exfoliating commercial expandable graphite by heating, dispersing it in a polymer solution via sonication, and then depositing GNRs from the supernatant [193].
- ***Artificial defect patterning and hydrogen-plasma etching***: This approach can consistently achieve sub-10 nm wide GNRs with smooth zigzag edges [53].
- ***Scanning tunneling microscopy (STM) cutting***: This method allows for the fabrication of GNRs with precisely controlled crystallographic edge orientations [194].

I.4.4 Properties of Graphene Nanoribbons

I.4.4.1 Electronic Properties

Quantum confinement and edge effects dominate the electronic properties of graphene nanoribbons [195]. Unlike pristine graphene, which is gapless, GNRs exhibit a finite and tunable bandgap inversely proportional to ribbon width [196]. Armchair-edged GNRs typically exhibit semiconducting behavior suitable for transistor applications, while zigzag edges exhibit metallic edge states with potential magnetic properties [197]. This tunability overcomes graphene's intrinsic zero-bandgap limitation, making GNRs attractive for digital electronics that require effective switching behavior [198,199]

I.4.4.2 Mechanical Properties

GNRs retain the exceptional tensile strength and flexibility of graphene despite their reduced dimensions. Their mechanical robustness makes them suitable for flexible electronics and nanomechanical systems [198] However, edge irregularities can influence mechanical performance, underlining the importance of precise fabrication techniques for applications demanding mechanical durability [199].

I.4.4.3. Thermal Properties

Graphene nanoribbons possess excellent thermal conductivity along their length, which facilitates efficient heat removal in nanoscale devices. Nevertheless, in narrower ribbons, thermal conduction is hindered due to enhanced phonon scattering caused by edge effects and defects. To address these challenges, improved fabrication methods and surface treatments have been introduced to reduce scattering and optimize thermal performance in graphene-based electronics [200, 201].

I.4.4.4 Optical Properties and Excitonic Effects

Graphene exhibits unique optical absorption of about 2.3% per monolayer across a broad spectral range (visible to near-infrared), resulting from the fine-structure constant and its constant optical conductivity [202]. The ultrafast carrier dynamics with relaxation times on the order of picoseconds enable applications in ultrafast photodetectors, modulators, and saturable absorbers [203]. Large nonlinear susceptibilities support frequency conversion and nonlinear optics [204]. Graphene nanoribbons (GNRs) have different optical properties than graphene due to unique structural features and size limitations. Unlike bulk graphene, GNRs show tunable optical responses based on their width, edge type, and even external electric fields. This gives rise to distinct optical phenomena which can be exploited for multiple purposes.

The Optical Properties of Graphene Nanoribbons (GNRs) and Their Structural Impact

I.4.4.5 Edge Types: GNRs can be differentiated into zigzag and armchair types with each possessing distinct optical properties. For instance, zigzag GNRs have a sharply increasing refractive index under an electric field. On the other hand, armchair GNRs have notable changes in conductance [205].

I.4.4.6 Chirality: GNRs that are chiral deviate from the conventional GNR model. Their broken symmetries have the effect of modifying absorption peaks and altering dielectric constants [206].

I.4.5 Applications in Optoelectronics

With the advancements in the technology involving GNRs, micro and nano optoelectronic devices and photodetectors as well as plasmonic devices have already started showing their potential. Their advanced utilization in electronic systems is a byproduct of the increased

versatility gained by GNRs due to the doping and electric fields. [207,208]. With the exceptional optical elements of GNRs, serve a wide array of functions photodetectors and plasmonic devices as well. Hence, one may appreciate the vast scope of research and applications of graphene based two dimensional structures. Due to their distinctive quantum and edge-derived properties, graphene nanoribbons are poised to become foundational materials for next-generation nano-electronic and optoelectronic devices. Advances in synthesis and functionalization will further unlock their potential across a range of technologies.

I.5. Conclusion

This chapter has established a comprehensive foundation by examining the diverse allotropes of carbon, emphasizing their structural variations and intrinsic properties. It has detailed the exceptional characteristics of carbon nanotubes, including their unique structure and physicochemical properties, while critically reviewing key synthesis methods. Additionally, the chapter introduced graphene nanoribbons, focusing on their distinctive electronic properties and synthesis challenges. By presenting the structure-property relationships and current fabrication techniques, this chapter provides a unified framework that underpins the more detailed experimental and theoretical analyses explored in subsequent chapters.

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II. Introduction

Although MOSFETs have been the cornerstone of electronic devices for decades, the relentless scaling down of their dimensions has pushed them toward fundamental physical and operational limits, threatening their continued dominance in future nanoelectronics [1]. This miniaturization, while enabling greater device density and performance, introduces critical challenges related to short-channel effects, leakage currents, heat dissipation, and variability in device characteristics, especially as devices approach the sub-10 nm regime [2]. These challenges have prompted intense research into alternative nanoelectronics device architectures that could sustain and surpass the performance of traditional MOSFETs. Among the promising candidates that have emerged are single-electron transistors and resonant tunneling devices, which exploit quantum mechanical phenomena such as Coulomb blockade and resonant tunneling to potentially achieve ultra-low power consumption and high-speed operation [3-4]. Concurrently, MOSFETs themselves continue to evolve with innovative designs to meet scaling requirements, but the practical and fundamental limitations at the nanoscale remain daunting [5].

In parallel, Carbon Nanotube Field Effect Transistors (CNTFETs) have gained remarkable attention due to their exceptional electrical, thermal, and mechanical properties. Since the first experimental demonstration of CNTFETs by Dekker and colleagues in 1998, significant advancements have been made, enabling devices that operate similarly to CMOS transistors with high current density, excellent switching behavior, and competitive transition frequencies [6]. Experimental CNTFET circuits have demonstrated high-frequency operation beyond 30 GHz, and fabrication techniques that achieve aligned and well-ordered carbon nanotube arrays have brought practical realization of these devices closer to reality. This chapter begins by presenting the structure, fundamental operating principles, and key characteristics of field-effect transistors, with an emphasis on MOSFETs and the miniaturization challenges they face. We then survey emerging nanoelectronics devices including single-electron transistors and resonant tunneling devices, highlighting their operational principles and advantages. Subsequently, a detailed focus is placed on CNTFETs, exploring their various types, structural configurations, fabrication techniques, and performance metrics. By integrating these perspectives, this chapter aims to provide a comprehensive foundation for understanding the evolving landscape of nanoelectronics and the potential role of CNTFETs as successors to traditional transistor technologies.

II.1 Introduction to Nanoelectronics Devices

Due to the ongoing miniaturization of MOSFETs and electronic devices, traditional MOSFETs are becoming inadequate in fulfilling their intended functions. As a result, researchers are investigating alternative device architectures to supplant conventional MOSFETs. Some of the primary contenders being evaluated for this transition are:

a) *Single-electron transistors*

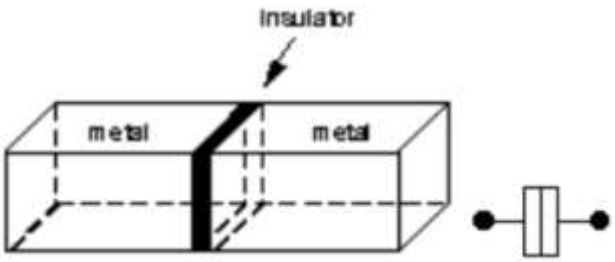
b) *Resonant tunneling devices*

c) *MOSFETs smaller than 10 nm*

d) *Carbon Nanotube Field Effect Transistors (CNFETs)*

II.2 Single-Electron Transistors (SET)

A team of Japanese researchers at NIST has successfully created logic circuits using single-electron transistors. These transistors are made of silicon nanowires measuring around 360 nm in length, each equipped with three insulating gates positioned at right angles. By applying a control voltage to these gates, the transistors can function as electronic switches, enabling precise regulation of electrical charge by manipulating individual electrons. The device described is a single-electron transistor (SET). It comprises a central conductive island isolated by tunnel barriers from the source and drain electrodes, with the potential controlled through a gate electrode. Owing to its extremely small geometric dimensions, the capacitances between electrodes in this device are exceptionally low.



(a) (b)

Figure II.1. *Schematic diagram of a tunnel junction [8].*

SETs function as switching devices that leverage controlled electron tunneling to modulate and amplify current. The fundamental architecture of a SET, illustrated in **Figure II.1**, features two tunnel junctions arranged in series, sharing a common electrode [7]. The tunnel junction, composed of two metallic pieces that are separated by an extremely thin insulator, demonstrates an inherent electrical capacitance resulting from its unique geometric

configuration. This capacitance is predominantly influenced by the specific dimensions and layout of the tunnel junction. Electrons traverse from one metal electrode to the other by means of tunneling through the insulating material, thereby facilitating the flow of electrical current.

The schematic representation of a single-electron transistor with a Coulomb island in the oxide is shown in **Figure II.2**.

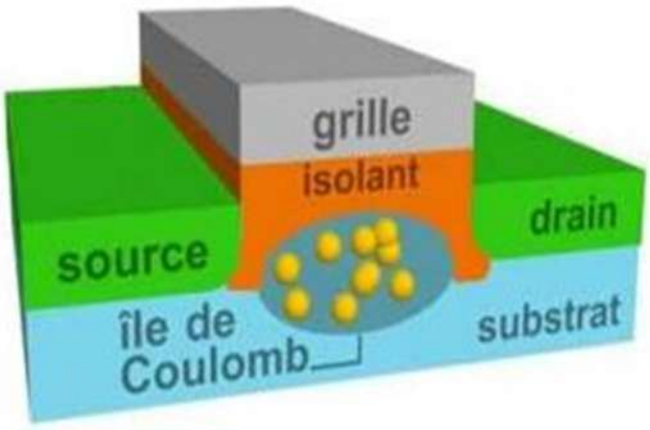


Figure II.2. *presents a schematic illustration of a single-electron transistor highlighting a Coulomb island embedded within the oxide layer [8].*

The fundamental building block of single-electron devices and circuits involves arranging two tunnel junctions in series to create a SET (see **Figure II.3**). The island is formed through capacitive coupling between the gate capacitance (C_g) and the node positioned between the two junctions [9]. The configuration of the circuit bears strong similarities to that of a three-terminal field-effect transistor. In this setup, the island takes on the role of the gate terminal, the drain terminals are symbolized by the node connected to the power supply, and the grounded node functions as the source terminal. The unique characteristics of each tunnel junction are defined by their respective capacitance values, labeled as C_1 and C_2, as well as their tunnel resistance values, denoted as R_1 and R_2.

Coulomb blockade is a phenomenon commonly observed in single-electron transistors (SETs) in which the tunneling process is hindered by the presence of a charge energy barrier. This Coulomb charging energy creates an effective energy gap, thereby impeding the flow of electrons until a requisite voltage is applied to surmount the barrier. Subsequently, upon the [10,11]. Entry of an electron into the island, a fresh instance of Coulomb blockade materializes, restricting the influx of further electrons until the previously introduced electrons vacate the island.

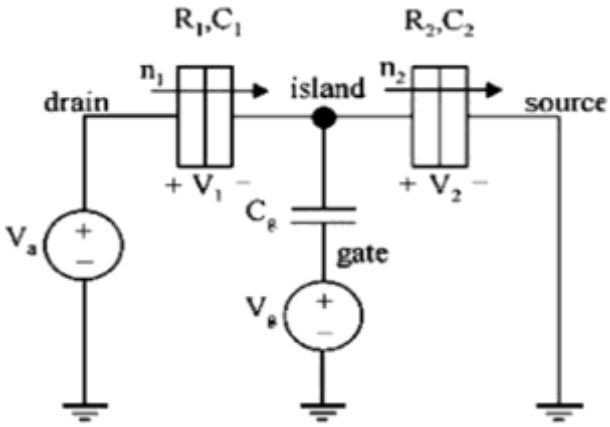


Figure II.3. *Schematic representation of a single-electron transistor (SET) circuit illustrating the flow of single electrons through the device [8].*

II.3 Resonant Tunnel Devices

Resonant tunnel devices are components that exploit quantum effects in their most fundamental form. The simplest type of resonant tunnel device is the resonant tunneling diode (RTD). The RTD is composed of alternating layers of two distinct III-V semiconductor alloys, typically GaAs and AlAs. An illustration of the RTD structure is provided in **Figure II.4** below [12].

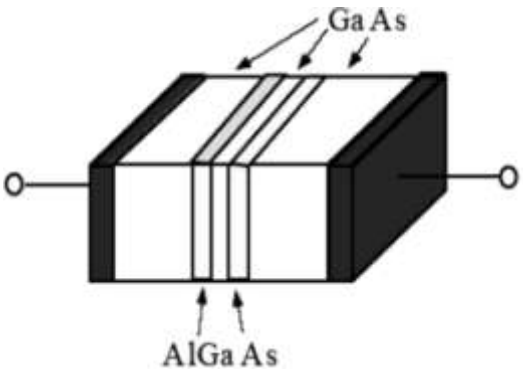


Figure II.4. *Structure of the resonant tunneling diode (RTD) [8].*

Figure II.5 illustrates the operation of the RTD. When an electron is confined within an island approximately 10 nm wide, quantum mechanics restricts its energy to discrete, quantized levels. This principle forms the foundation of RTD functionality. Electron flow occurs through quantum mechanical tunneling across the two barriers. Tunneling is possible only if the electron's energy matches one of the quantized energy levels within the island; otherwise, no current flows, and the device remains in a blocked state. Whenever the incoming electron's

energy aligns with the island's energy level, current pass, and the device stays in an active state [12].

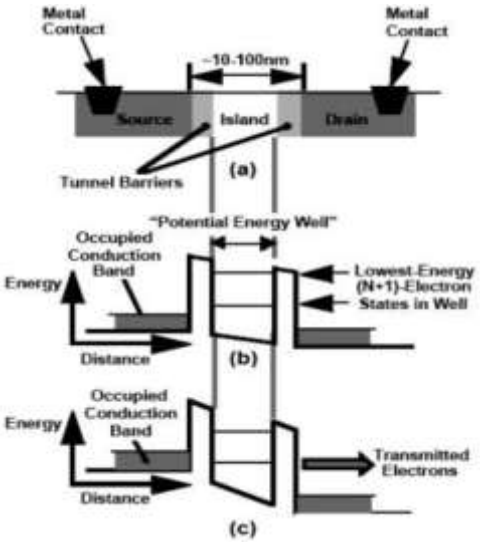


Figure II.5. *(a) Schematic diagram of the resistance probe structure, (b) probe in the blocked state, (c) probe in the conducting state [8].*

Figure II.6 presents the current voltage characteristics of the RTD. Initially, due to electron tunneling, the current rises as the voltage V_d increases. However, beyond a certain voltage threshold (I_{ON}), electrons from the left can no longer tunnel into the well, causing the current to decrease. If V_d continues to increase further, the current begins to rise again, driven by thermal effects. The term I_{ON} refers to the maximum peak current generated by the process of electron tunneling, while IVALLEY represents the minimum valley current that is produced because of the decrease in tunneling activity. A higher ratio of I_{ON} to IVALLEY is typically more desirable as it indicates a greater level of amplification. Additionally, this elevated ratio often correlates with a lower IVALLEY, which is advantageous as IVALLEY is commonly associated with leakage current, and decreasing it results in lower power consumption [13].

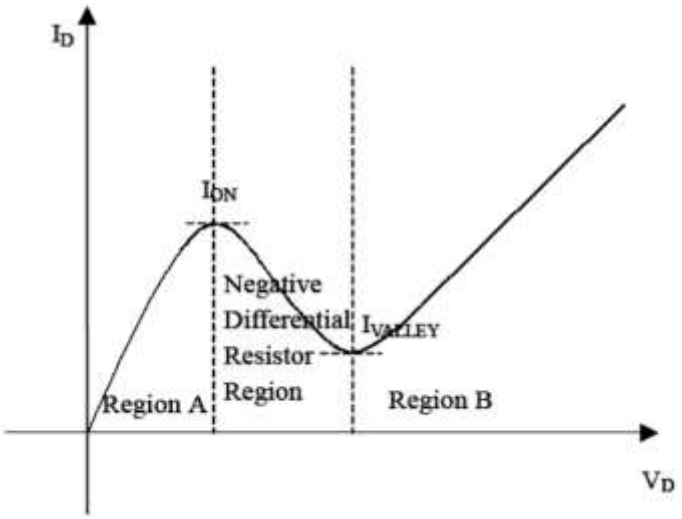


Figure II.6. *I-V characteristics of the RTD [8].*

II.4 Definition and Types of FET

The concept of the physical principle behind field-effect transistors (FETs) was theoretically proposed by William Shockley in 1952 [14] when he published his work on the junction field-effect transistor (JFET). A field-effect transistor is a unipolar device in which only majority charge carriers participate in its operation. Because electrons possess the most favorable transport properties such as mobility, velocity, and diffusion coefficient, the FETs that are commonly manufactured are primarily of the N-type. There are mainly three FET structures, each corresponding to different gate contact configurations:

- PN junction gate for the Junction Field Effect Transistor (JFET).
- Metal gate with a Schottky barrier for Metal-Semiconductor Field Effect Transistor (MESFET) and High Electron Mobility Transistor (HEMT).
- Insulated metal gate for Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and Metal-Insulator-Semiconductor Field Effect Transistor (MISFET). Shockley's 1952 theoretical proposal followed earlier foundational concepts by Julius Lilienfeld (1925 patent) and the practical creation of working FET devices by others such as George Dacey and Ian Ross in 1953. This development paved the way for diverse FET technologies used widely in modern electronics [15].

II.5 MOSFETs Smaller than 10 nm

MOSFETs with gate lengths below 10 nm belong to a class of nanoelectronic devices that remain compatible with existing fabrication processes and design methodologies. This type

of device has been extensively studied through simulations, as evidenced by numerous research efforts. Among these studies, many have focused on ballistic MOSFETs, which feature a double-gate design. While their overall structure is similar to conventional MOSFETs, the source and drain regions in ballistic MOSFETs are composed of silicide or metal instead of heavily doped semiconductor material [16] The structure of the SBFET (Schottky Barrier Field-Effect Transistor) is shown in **Figure II.7.**

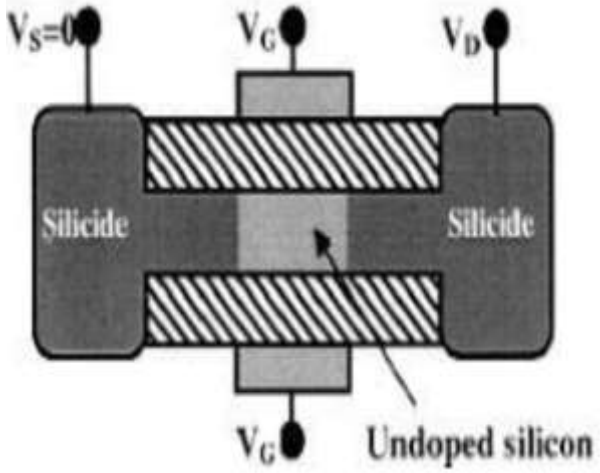


Figure II.7. *Dual-gate Schottky Barrier Field-Effect Transistor (SBFET) [16].*

The Schottky Barrier Field Effect Transistor (SBFET) offers notable advantages in both manufacturing processes and device performance. From a fabrication perspective, the SBFET removes the necessity for extremely high doping levels in the source drain regions a challenging requirement at the nanoscale. In terms of performance, SBFETs are capable of delivering higher current output while simultaneously exhibiting significantly reduced leakage currents. Simulation based studies have shown that the operating characteristics of SBFETs closely resemble those of traditional MOSFETs when the Schottky barrier height is lowered [16]. This suggests that achieving a negative Schottky barrier is crucial for obtaining high current gain in SBFET devices. An alternative simulation method for Schottky Barrier MOSFETs (SBMOSFETs) involves the use of metallic filters. In this approach, source and drain regions are composed of a specific material combined with an intrinsic substrate to isolate neighboring electrodes effectively [17]. In summary, tunnel Field Effect Transistors (FETs are less affected by short-channel effects, making them promising candidates for scaling down below the 10-nanometer regime. However, these tunnel FETs require a fully intrinsic substrate since doping cannot reliably control transistor characteristics at such minuscule scales.

II.6 Carbon Nanotube Field-Effect Transistor (CNTFET)

Among the most promising devices in nanoelectronics is the carbon nanotube field-effect transistor (CNTFET), recognized for its excellent electrical properties. Its design closely resembles that of a MOSFET, with the key difference being the substitution of the silicon channel by a semiconducting carbon nanotube. A cross-sectional diagram of the CNTFET structure is illustrated in **Figure II.8**.

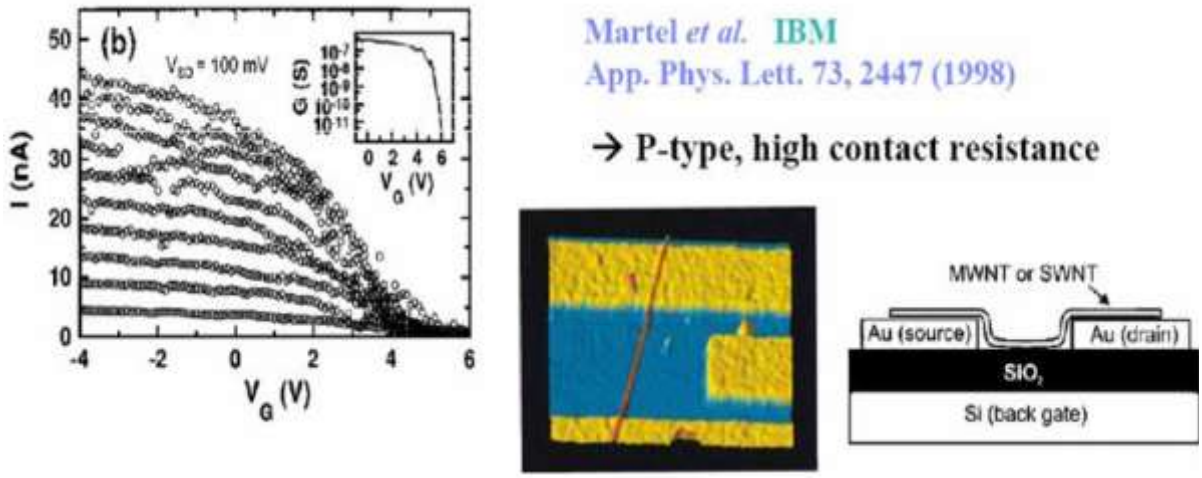


Figure II.8. *Initial design of a CNTFET [18].*

The first carbon nanotube field-effect transistors were demonstrated in 1998. These initial devices were simply made by depositing single-wall carbon nanotubes produced through laser ablation from a solution onto oxidized silicon wafers that had gold or platinum electrodes pre-patterned on them. The electrodes acted as the source and drain, connected by the nanotube channel, while the doped silicon substrate functioned as the gate. A schematic representation of this device is provided in **Figure II.8**. The devices exhibited clear p-type transistor behavior, with the drain current modulated by the gate voltage across several orders of magnitude. However, they showed relatively high on-state resistance in the megaohm range, low transconductance (around micro-Siemens), lacked current saturation, and required relatively high gate voltages several volts to activate [19].

II.6.1 Types and Operating Principles of CNTFETs

Since the introduction of the first carbon nanotube field-effect transistor (CNTFET), various types of CNTFETs have been developed. Subsequent improvements have focused on enhancing carrier transport within the carbon nanotube channel to achieve optimal efficiency. These transistor types include barrier-height-modulated CNTFETs and dual-gate CNTFETs. Additionally, phototransistors based on CNTFET technology, such as optically gated

CNTFETs, have also been realized. These different CNTFET variants primarily differ in the gate structure design and the nature of the current transport mechanism, which can be either tunneling or thermionic. This section presents these CNTFET types while explaining their respective operating mechanisms [21].

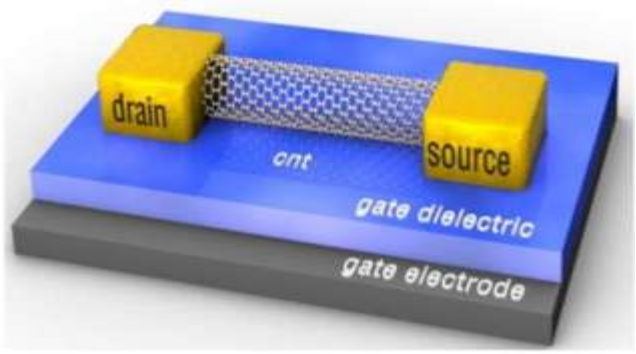


Figure II.9. *Transistor with a CNT as the channel [20].*

II.6.1.1 Operating Principle

A conventional CNTFET operates in a manner similar to a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). In a CNTFET, the carbon nanotube acts as the conductive channel, enabling partially ballistic transport. **Figure II.10** illustrates electron transport and the associated wave vector vectors in an N-type CNTFET. In this figure, both the drain and source contacts are assumed to be ohmic contacts interfacing the CNT channel. The electrical potential along the channel is modulated by the gate voltage, which controls the flow of electrons through the CNT, allowing or blocking current conduction [22]. This transistor is commonly referred to as a barrier-height-modulated CNTFET or MOS-like CNTFET due to its behavioral similarity to a conventional MOSFET.

However, electron transport in the CNTFET differs significantly from that In MOSFETs, this is due to a high ballisticity rate, which occurs when the channel length is equal to or shorter than the electron means free path [23]. Specifically, for N-type CNTFETs, electrons are injected from both the drain and source terminals, contributing to the ballistic current depending on whether the longitudinal wave vector is directed as -k or +k, respectively. In other words, both contributions share the same nature but with opposite directions. An analogous principle applies to P-type CNTFETs, where hole transport occurs within the valence band.

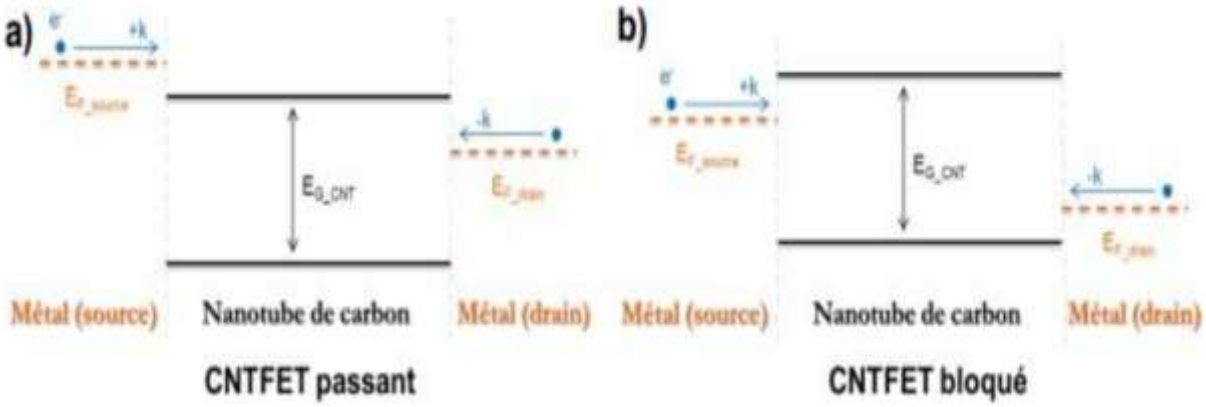


***Figure II.10**. Energy diagrams of an N-type MOS-like CNTFET under two bias conditions showing: the on-state (a) and the off-state (b). The V_{ds} bias is positive in both cases. In (a), V_{gs} is highly positive, while in (b), it is slightly positive [24].*

A fabrication process similar to the planar process used for MOSFETs is illustrated in **Figure II.11(a). The** carbon nanotube channel is created by deposition rather than epitaxy, as is the case in the CMOS (Complementary MOS) process (**Figure II.11(a)1**). This is followed by the deposition of the drain and source electrodes (**Figure II.11(a)2**). The type of contact (N or P) is determined by the metal used and the diameter of the CNT. Notably, in an n-FET design, the electrodes are made of aluminum, while in a p-FET, gold electrodes are used. Self-alignment defines the channel after the lift-off step. The gate dielectric is locally deposited using the Chemical Vapor Deposition (CVD) method (**Figure II.11(a)5**). Subsequently, the gate metal is deposited (**Figure II.11(a)6**), and self-alignment after lift-off is employed to form the gate electrode (**Figure II.11(a)7**). This method leads to the formation of a "front gate." The back gate, typically fabricated from silicon heavily doped with aluminum, is created before the oxide layer, which is grown in situ. The simplicity of this process grants CNTFET compatibility with CMOS technology [24].

To simplify the CNTFET fabrication process and thereby reduce its cost, the channel is predominantly kept free of any dopants. Furthermore, the absence of dopants is desirable to minimize variability. Although oxygen is not truly a dopant for carbon nanotubes, it does influence the metal/semiconductor contact properties by enhancing hole transport [26]. Using metals with a work function higher than that of the CNT facilitates the realization of P-type CNTFETs (without passivation) [27,28]. The fabrication of N-type transistors is achievable by removing oxygen from the CNT channel through vacuum annealing with passivation and selecting metals having a work function lower than that of the CNT [28,29]. The quality of control between the on and off states is characterized by the subthreshold slope inverse in the

I_{DS}-V_{GS} characteristics of the FET transistor. The lower this value, the steeper the I_{DS}-V_{GS} curve, resulting in better-defined ON/OFF levels and improved transistor performance. The best P-type CNTFET measured to date exhibited a subthreshold slope inverse of 85 mV/decade [30]. The transition time, or cutoff frequency, is considered another key advantage. A ring oscillator operating at a resonance frequency of 52 MHz was demonstrated, achieving a transition time of 1.9 ns per stage. As another example, a CNTFET reached a cutoff frequency of 80 GHz with a channel made of non-aligned SWNT networks [31].

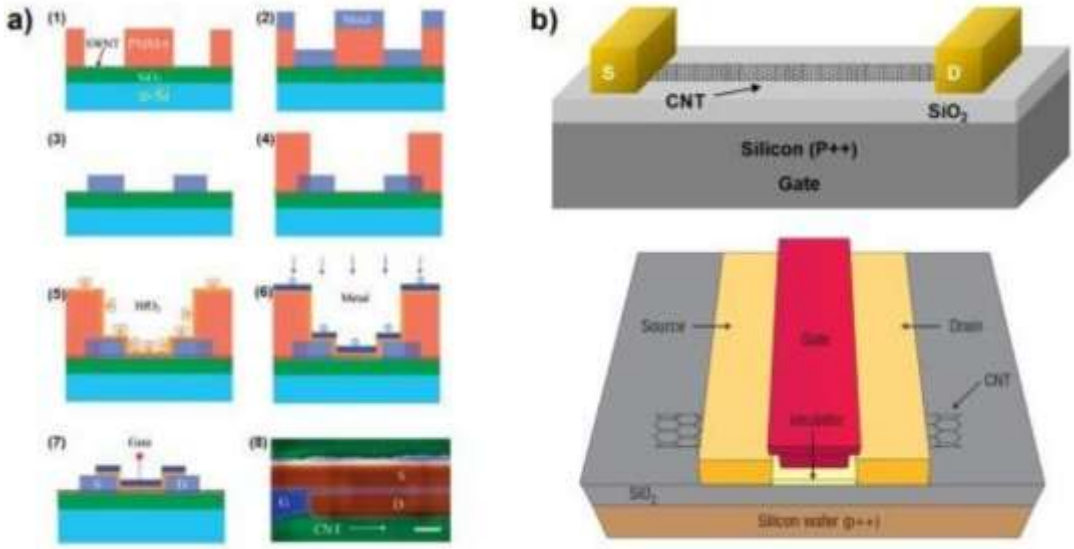


Figure II.11. *(a) Self-aligned fabrication process of a "top-gate" CNTFET using an HfO_2 gate oxide [25], (b) schematic configuration of CNTFETs featuring a back gate at the top and a top gate at the bottom [26].*

Figure II.12 presents implementations of CNTFETs with a single semiconducting carbon nanotube. Currently, this type of device remains primarily a laboratory demonstration. Regardless of the fabrication method used whether depositing single-wall carbon nanotubes (SWNTs) on a substrate by spin-coating or localized growth no technique has yet been developed to produce large numbers of transistors each containing only a single nanotube for achieving high integration density. Most often, the channel consists of a network of CNTs that are more or less aligned. Nevertheless, this component has been extensively studied, and numerous compact models have been developed to meet the requirements for integrated circuit design [32–36]. Furthermore, simple circuits have been realized using conventional CNTFETs.

A logic gate, specifically an inverter, has been fabricated [37,27] (**Figure II.12a**). Additionally, a five-stage ring oscillator based on CNTFET inverters was developed (**Figure II.12b**).

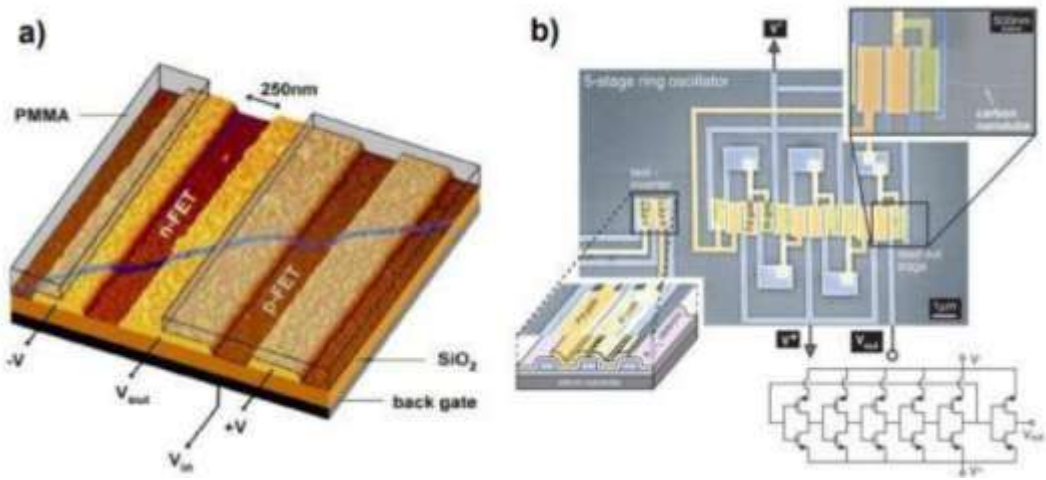


Figure II.12. *(a) Illustration of the inverter using two types of CNTFETs: a p-CNTFET and an n-CNTFET [38]. (b) Image of the five-stage ring oscillator circuit [39].*

II.6.1.2 Different Types of CNTFETs

a) Barrier-Height Modulated Transistors (C-CNTFET)

The carbon nanotube field-effect transistor with barrier height modulation, also known as the conventional CNTFET (C-CNTFET), is fabricated using a single-wall carbon nanotube with n/i/n or p/i/p doping profiles [40,41]. It closely resembles a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), with the key difference being the replacement of the channel material by a carbon nanotube to leverage ballistic transport in CNTs (**Figure II.13**). Due to its behavioral similarity to the MOSFET, this transistor is often referred to as a MOS-like CNTFET. However, carrier transport in the CNTFET differs from that in the MOSFET: under conditions where the channel length is less than or comparable to the electron means free path, electron transport in the CNTFET exhibits a high ballistic mode rate exceeding 80% [42,43]. The contact between the metal electrodes (source or drain) and the nanotube is assumed to be ohmic or have a low barrier height [44,45], which represents an improvement over Schottky barrier nanotube transistors. The nanotube ends near the source and drain contacts serve as carrier injection points, while the internal region, whose energy band positions are modulated by the gate bias, controls the passage or blocking of carriers.

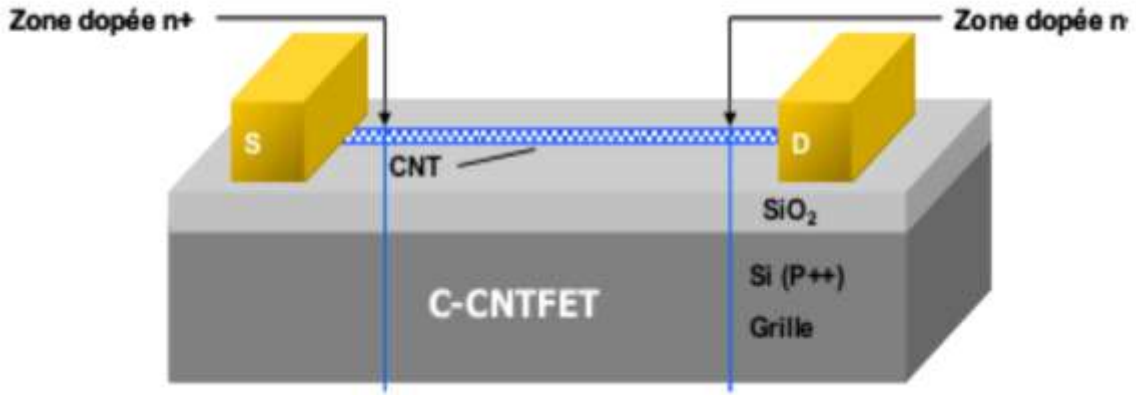


Figure II.13. *Cross-sectional view of the barrier-height modulated CNTFET or C-CNTFET [24]*

b) Schottky Barrier CNTFET (SB-CNTFET)

A carbon nanotube transistor consists of two metal/nanotube contacts at the source and drain sides. The metal can be aluminum (Al), titanium (Ti), palladium (Pd), or scandium (Sc), while platinum (Pt) is rarely used because it has poor wettability with carbon nanotubes [46]. that is, it exhibits low adhesion energy. At the interfaces formed between the metal contacts and the semiconducting nanotube, Schottky potential barriers are created, which oppose the transport of carriers between the source and drain through the nanotube channel. Thus, these barriers play a significant role in determining the current, as they govern the number of carriers present on the metal side and transmitted into the channel [47]. To highlight the presence of these Schottky barriers in carbon nanotube transistors, Freitag et al. [48] observed them using two different microscopy techniques: Scanning Gate Microscopy (SGM) [49] and Scanning Photocurrent Microscopy (SPCM) [35]. The height of the Schottky barrier results from the difference between the metal work function and the nanotube's electron affinity, which depends on its chirality (or diameter). To establish a direct relationship between the Schottky barrier height and the metal and nanotube work functions, it is preferable to use mid-gap Schottky barrier heights.

In a barrier-height modulated CNTFET, it is the nanotube channel potential, denoted here as $\Phi^0{}_f$, that determines the current flow in the channel at the metal/nanotube interface. Electrons with energy greater than $\Phi^0{}_f$ contribute to the total current. A variation in gate potential changes the channel potential and modulates the number of carriers contributing to the current [52]. In the case of SB-CNTFETs, the situation is different: a change in gate potential modifies the channel potential $\Phi^0{}_f$ but also alters the shape of the Schottky barriers at the source and drain, which control carrier injection (**Figure II.14**). A change in gate or drain bias

alters the channel potential Φ^0_f but also varies the dimensions (height and width) of the two Schottky barriers. In general, the energy band profile near the contact strongly depends on the biases and (**Figure II.15**).

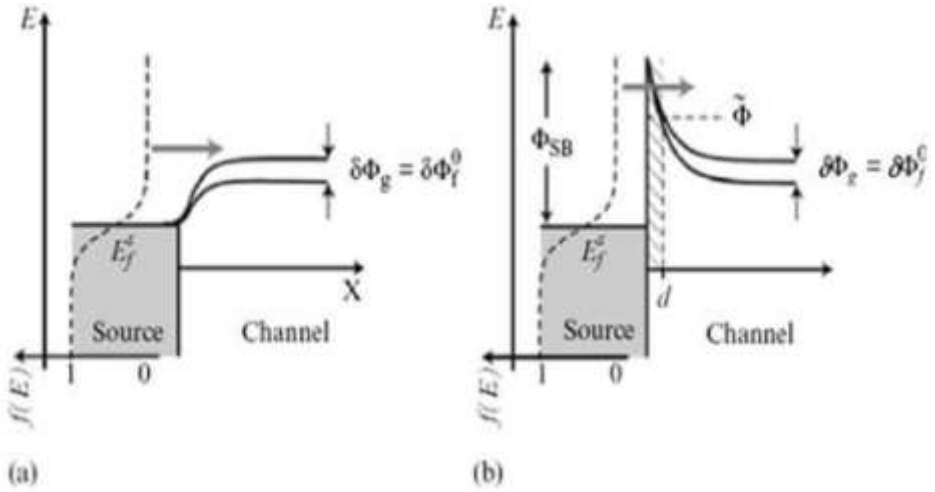


Figure II.14. *Conduction band profile for a C-CNTFET (a) and for an SB-CNTFET (b), showing the variation of the surface potential as a function of the applied gate voltage [51].*

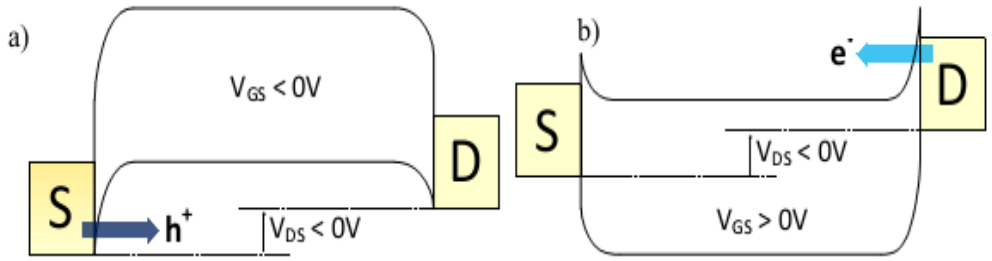


Figure II.15. *Energy band diagrams explaining, for the same V_{DS}, (a) the P-type behavior resulting in hole current (negative V_{GS}), (b) the N-type behavior resulting in electron current (positive V_{GS}) [24].*

In the following **Figure II.16,** we present a structure of a SB-CNTFET in a "back-gate" configuration, and then in **Figure II.17** we present an energy band diagram (without Schottky barriers) of the C-CNTFET transistor along the source-drain axis for $V_{GS} = 0$ V and $V_{DS} > 0$ V. $E_{F,S}$ and $E_{F,D}$ are the Fermi levels of the source and drain metals, respectively [49,53].

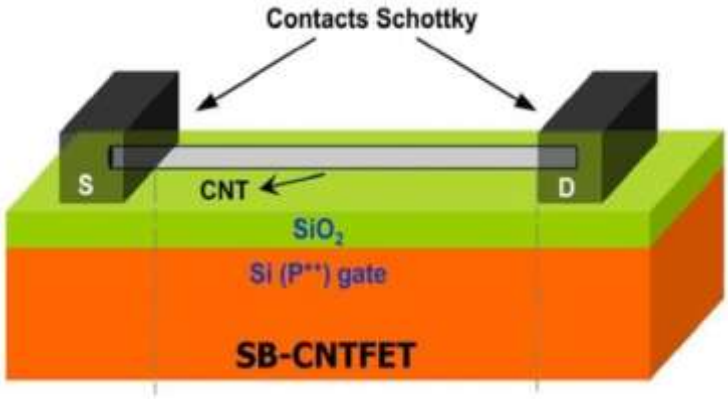


Figure II.16. *Structure of a SB-CNTFET [53].*

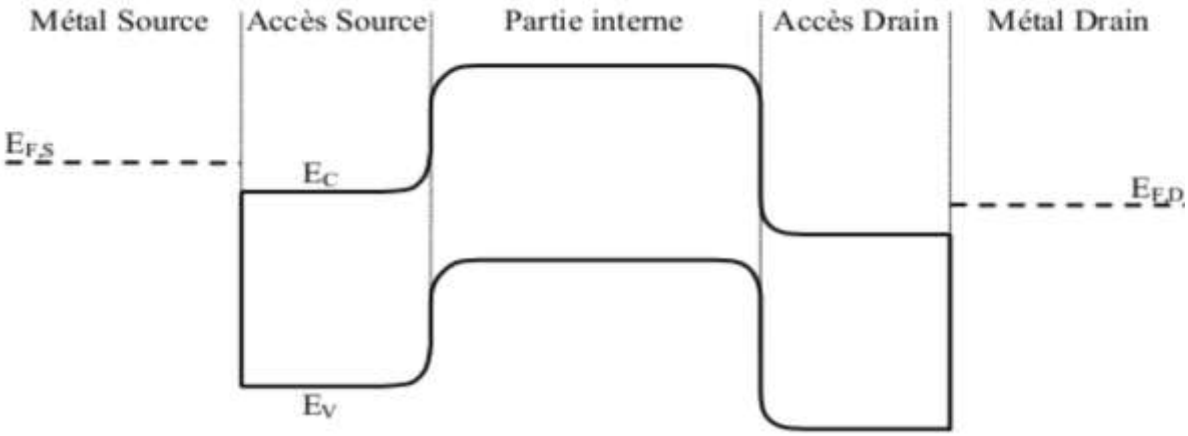


Figure II.17. *Schematic representation of the energy bands of the C-CNFET transistor along the source-drain axis for V_{GS}= 0 V et V_{DS}> 0 V.*

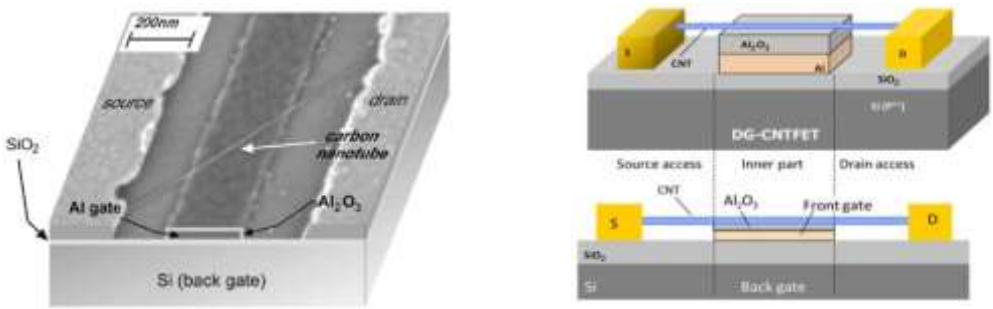
An example of a fabrication process intended to be close to the planar process used for MOSFETs [54]. The CNT channel is created by deposition instead of epitaxy in the CMOS (Complementary MOS) process. Then, the drain and source electrodes are deposited. Depending on the nature of the metal and the diameter of the nanotube, the contact is either N-type or P-type. For example, aluminum (Al) electrodes are used in an n-FET implementation Another example is gold (Au) electrodes used in a p-FET. The gate dielectric is locally deposited by CVD. Then the gate metal is deposited [55].

c) Double-Gate Transistors (DG-CNTFET)

The Double-Gate CNTFET (DG-CNTFET) features an additional front gate positioned between the source and drain contacts, beneath the carbon nanotube [26]. A thin insulating layer of approximately 4 nm separates this aluminum front gate from the nanotube. The operating

principle of this transistor type relies on electrostatically doping the access regions to create an n/i/n or p/i/p configuration, similar to the barrier-height modulated CNTFET (**Figure II.18.a**). This electrostatic doping of the nanotube's access regions is achieved by the electric field generated from the back gate bias, while the inner channel region is screened by the front gate. Double-gate field-effect transistors can be designed either with a nanotube channel or a silicon channel. An example of a "gate-all-around" (GAA) double-gate FET is shown in **Figure II.18.b** [56]. However, it is technologically challenging to fabricate silicon transistors operating in the ballistic regime because the electron means free path is less than 20 nm at room temperature. In these cases, lithography limits the deposition and etching of the second gate. In contrast, due to the high mean free path in carbon nanotubes, it is entirely feasible to design logic circuits using double-gate CNTFETs. A prototype has been developed with a 100 nm channel length and a 40 nm front gate [57].

The most recent advancement in CNTFET technology could be the initiation of the vertical CNTFET. This gate structure was introduced by Choi et al. in 2004 [59], inspired by IBM's model of vertical transistors. The concept of vertical CNTFETs made three dimensional circuits feasible. In this case, the size of the CNTFET can be as small as the diameter of the carbon nanotube, corresponding to an integration density of 10^{12} elements per cm^2.



(a) *(b)*

Figure II.18. *Cross-sectional view of the Double-Gate CNTFET (DG-CNTFET) (a) [56], (b) [58].*

d) Vertical-gate CNTFET (V-CNTFET)

The vertical CNTFET is fabricated as follows: formation of nanopores by anodization, followed by synthesis of the carbon nanotube, formation of metal electrodes, deposition and patterning of oxides, and finally formation of the gate electrode. Silicon oxide is deposited on

top of an aligned carbon nanotube by evaporation using an electron gun, followed by the formation of holes via electron beam and chemical etching. The oxide deposition process is then followed by the deposition of the upper gate electrode [60-61].

The structure of the vertical CNTFET is shown in **Figure II.19**.

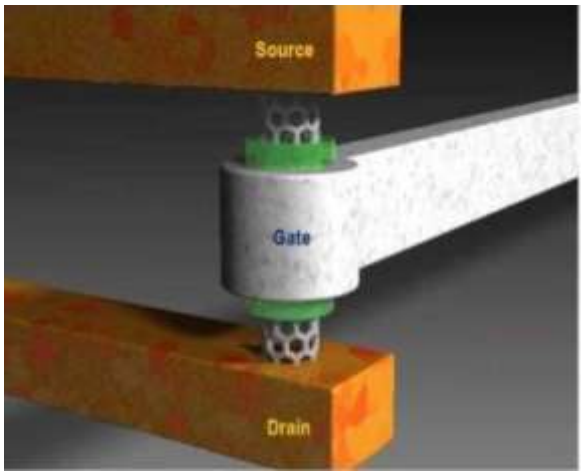


Figure II.19. *Vertical CNTFET (presented by Infineon Technology in November 2003).*

The processes used to fabricate a vertical CNTFET are illustrated in **Figure II.20** [26]. In this structure, each carbon nanotube is electrically connected to the lower electrode (the source), the upper electrode (the drain), and the gate electrode, which is placed around the carbon nanotube. Each intersection points of the source and drain electrodes corresponds to a transistor element containing a single vertical carbon nanotube.

e) Optically Gated Transistors (OG-CNTFET)

The OG-CNTFET device is developed based on a CNTFET structure featuring a p-type back gate. The gate dielectric comprises silicon dioxide, formed through localized thermal oxidation, which ensures a high-quality dielectric layer confined to the desired areas. A thin film of poly(3-octylthiophene) (P_3OT), approximately 5 nm thick [63], is then uniformly applied over the entire wafer using a spin-coating method. Notably, P_3OT is a photosensitive polymer extensively employed in photovoltaic energy conversion applications [64-65]. Upon exposure to light, photogenerated electrons induce modulation of the OG-CNTFET channel, sustaining this modulation for durations extending beyond a full day. Consequently, this device functions simultaneously as an optoelectronic component and a form of non-volatile memory.

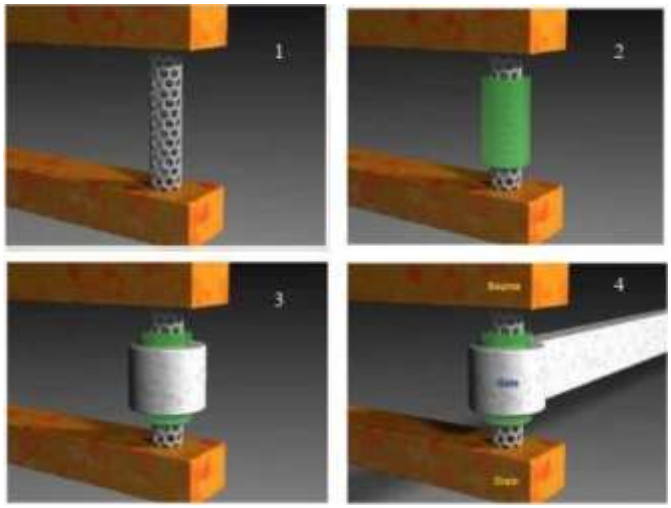


Figure II.20. *Fabrication process of a vertical CNTFET [62].*

II.6.2 Operating Principle of the Optically Gated Carbon Nanotube Field-Effect Transistor (OG-CNTFET)

The operational mechanism of the OG-CNTFET hinges on the interaction between incident photons and the photosensitive polymer layer incorporated within the device architecture. Upon exposure to illumination at a specific wavelength range, the polymer typically poly(3-octylthiophene) (P_3OT) undergoes photoexcitation, generating electron-hole pairs within its matrix [66]. Although the generation process yields a substantial number of charge carriers, empirical studies indicate that only a minor fraction, typically less than 5%, of the photogenerated electrons are effectively trapped in the polymer or at its interface with the gate dielectric (SiO_2). This trapping phenomenon is critically influenced by the electrostatic environment established by the gate electrode. In particular, when a positive gate bias (V_{gs}) is applied, the transistor is electrically turned off, creating an electric field that extends across the channel region and into the polymer/dielectric interface. This field acts to attract and localize the photogenerated electrons, causing their accumulation at the SiO_2 interface directly adjacent to the carbon nanotube channel. The presence of these trapped charges near the nanotube surface induces a modulation of the channel potential. This modulation arises from the local alteration of the electrostatic landscape governing carrier transport within the nanotube, effectively changing the threshold conditions for conduction. In consequence, the channel conductance can be modulated in a non-volatile manner, since the trapped charges persist over extended durations, enabling the device to function as both an optoelectronic transistor and a form of light-addressable non-volatile memory. Importantly, the spatial extent of this trapped charge distribution is confined to the illuminated region, enabling localized control of the

channel potential via optical stimuli. This unique coupling of optical and electronic control mechanisms highlights the versatility of the OG-CNTFET architecture for applications in photodetection, optoelectronic switching, and memory devices within nanoscale integrated circuits.

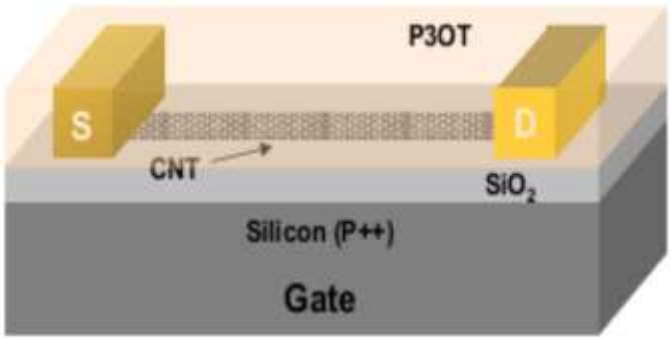


Figure II.21. *Schematic representation of an OG-CNTFET [67].*

Figure II.22 illustrates the energy band diagram and charge distribution scenario under illumination and positive gate bias, visually depicting the trapping sites and resultant channel modulation. Future work may investigate the dynamics of charge trapping and detrapping, the impact of polymer thickness and morphology on device performance, and the influence of different polymer materials with varied photoresponse characteristics to optimize the operational stability and efficiency of OG-CNTFETs [24], [66,67].

Indeed, the charge corresponding to these electrons is localized in close proximity to the gate electrode. Consequently, the modulatory influence of the gate is effectively screened by the presence of these trapped electrons. This phenomenon is referred to as “Optical Gating.” Notably, upon cessation of illumination, the trapped electrons do not recombine instantaneously; rather, the Optical Gating effect persists for a duration exceeding one full day [60].

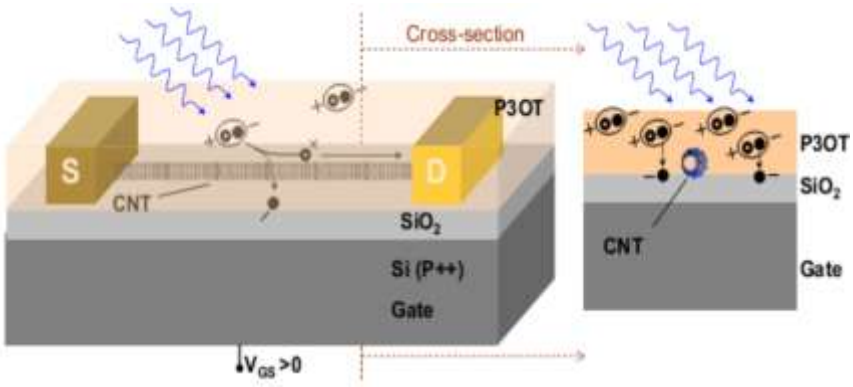


Figure II.22. *Schematic representation of the dynamics of the "Optical Gating" effect in an OG-CNTFET [68].*

II.7 Emerging Photonics Based on Carbon Nanotubes

Carbon nanotubes exhibit unique optical and optoelectronic properties that have garnered substantial attention within the scientific community. These nanostructures demonstrate strong luminescence upon optical or electrical excitation, as well as characteristic electro-absorption and electro-refraction effects. Such phenomena represent novel physical mechanisms at the nanoscale and hold significant promise for the advancement of photonic and photoelectric devices [69-70]. However, the optical characteristics of carbon nanotubes are inherently heterogeneous, and not all nanotubes are equally suitable for photonic applications. Therefore, it is essential to develop effective sorting and selection techniques to isolate nanotubes with optimal optical performance. Notably, specific subpopulations of nanotubes display optical gain, defined as the ability to amplify photon flux, marking a crucial milestone towards realizing carbon nanotube-based laser technologies [71-72].

II.7.1. New Optical Properties of Semiconducting Nanotubes

The assessment of the extraction quality of semiconducting nanotubes using PFO is conducted by comparing the optical properties of three thin-film samples: (i) raw nanotubes, (ii) nanotubes subjected to mild centrifugation (reducing the number of nanoparticles and metallic nanotubes), and (iii) purified semiconducting nanotubes. Several optical techniques can be employed to record photoluminescence spectra at varying excitation pump wavelengths. For nanotubes, the pump wavelength corresponds to the S22 transition energies, while the emission wavelength measured in photoluminescence pertains to the S11 transition energies. This photoluminescence mapping yields a distinct set of peaks, each identified by pairs of

excitation and emission wavelengths, which correspond to specific (S22, S11) transitions and therefore to a well-defined chirality (n, m) [73].

Following an incomplete extraction of semiconducting carbon nanotubes, a reduction in the variety of observed chiralities occurs, ultimately yielding two predominant chiralities specifically, the (8,6) and (8,7) nanotubes after complete extraction. The semiconducting nanotube extraction via polyfluorene (PFO) effectively corresponds to a selective sorting based on the chiral angle of the nanotubes. Indeed, both the (8,6) and (8,7) nanotubes possess chiral angles exceeding 25°, which results in an oblique wrapping of the hexagonal lattice of carbon atoms around the nanotube axis. This observation correlates strongly with the helical wrapping conformation naturally adopted by PFO when dissolved in solution. An important question remains: what is the influence of semiconducting nanotube enrichment on the photoluminescence intensity? **Figure II.23** presents the photoluminescence spectra of the three previously described thin films comprising PFO/nanotube composites, excited with a pump laser at a wavelength of 740 nm, which selectively probes only the (8,6) nanotubes. The concentration of (8, 6) nanotubes within each thin film was carefully adjusted to be equivalent across the samples to enable direct comparison.

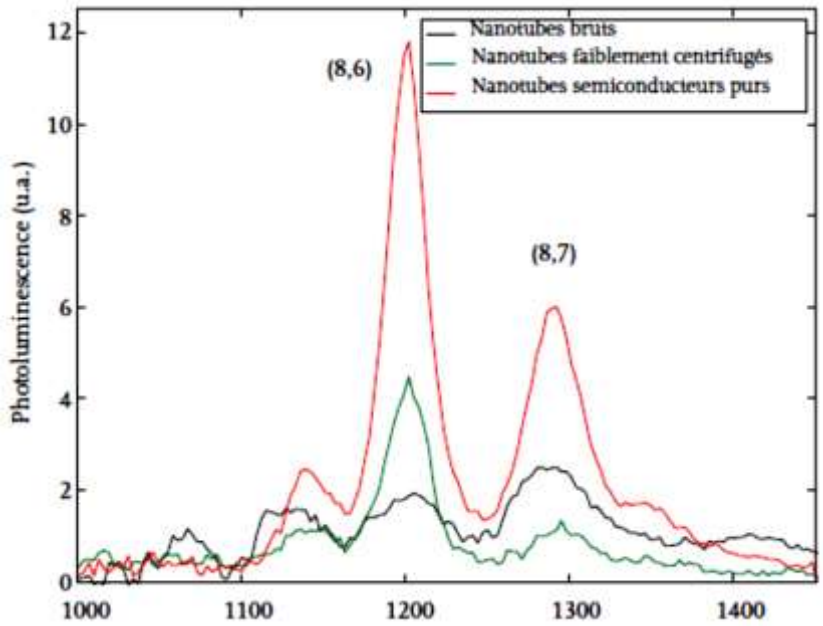


Figure II.23. *Photoluminescence intensities of the three nanotube samples as a function of their purification level [73].*

The effect of enrichment in semiconducting nanotubes which concomitantly corresponds to the depletion of metallic nanotubes is clearly evident in these spectra. Specifically, the photoluminescence intensity originating from the (8,6) nanotubes is enhanced by a factor of three compared to the semi-purified sample and by more than a factor of six relative to the non-purified sample. This enhancement in photoluminescence signal can be attributed primarily to the removal of impurities, including carbonaceous nanoparticles and metallic nanotubes, which are substantially present approximately one third by quantity in the non-purified samples. Metallic nanotubes provide undesirable non-radiative relaxation pathways for excitons generated within the semiconducting nanotubes, substantially quenching the photoluminescence. Therefore, their near-complete elimination in the fully purified sample suppresses these non-radiative channels, resulting in a pronounced increase in photoluminescence intensity [74].

II.7.2. Optical Gain

However, the precise role of the PFO matrix on semiconducting nanotubes for instance, as a protective layer against oxygen remains unclear, and investigations are ongoing. Nonetheless, it is well established that the presence of metallic nanotubes and nanoparticles is particularly detrimental to photoluminescence, and more broadly, to all optical properties associated with semiconducting nanotubes [75]. The experimental observations and schematic representations of this optical gain are depicted in **Figure II.24**.

II.7.3. Towards the Carbon Nanotube Laser

A thin film composed of sorted nanotubes containing exclusively semiconducting nanotubes exhibits photoluminescence properties that are significantly enhanced compared to the base sample. However, for carbon nanotubes to hold promise in photonic applications, they must demonstrate not merely good but superior properties relative to competing materials. This endeavor begins with the demonstration of optical gain in nanotube samples. Optical gain in a medium quantifies its ability to amplify the photon flux passing through it. It is a fundamental property required to achieve the laser effect. Explanations of optical gain measurement techniques are provided in Box 2. The investigation of optical gain was conducted by assessing two thin-film PFO/nanotube samples: the first, referred to as sample A, contains only semiconducting nanotubes (8,6) and (8,7)), whereas the second thin film, termed sample B,

comprises a mixture of semiconducting and metallic nanotubes. The optical gain results measured for these two films are presented in **Figure II.25**.

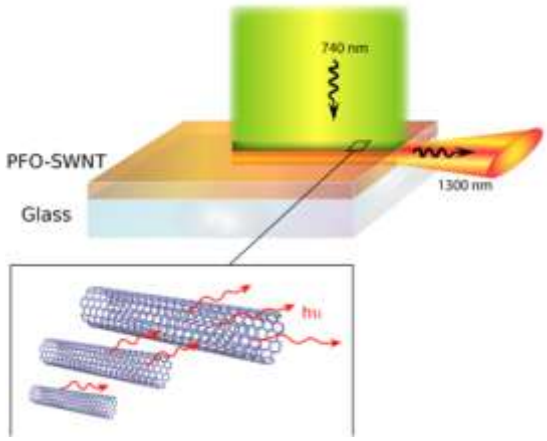
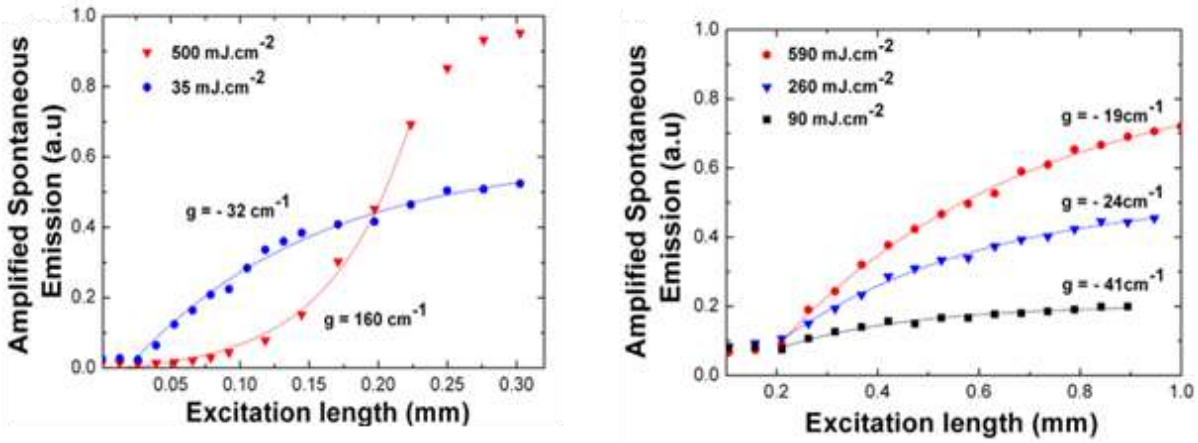


Figure II.24. *Optical Gain in Carbon Nanotubes (CNTs) [75]*



(a) (b)

Figure II.25. *Amplified spontaneous emission intensity as a function of the excitation beam length for different pump energies [75].*

Conclusion

This chapter has presented a thorough overview of the evolving landscape of nanoelectronics devices, emphasizing the constraints faced by traditional MOSFETs as device scaling approaches fundamental physical limits in the sub-10 nm regime. The discussion highlighted the critical challenges introduced by miniaturization such as short channel effects, leakage currents, and heat dissipation that necessitate exploration of alternative device architectures. A comprehensive survey of emerging nanoelectronics technologies was provided,

including single-electron transistors and resonant tunneling devices, which leverage quantum mechanical phenomena to achieve ultra-low power and high-speed operation. However, the primary focus of this chapter was to detail Carbon Nanotube Field Effect Transistors (CNTFETs) as promising successors to MOSFETs, given their superior electrical, thermal, and mechanical characteristics.

Importantly, this chapter concentrated on the state-of-the-art understanding and classification of CNTFETs rather than experimental fabrication or testing. It described various CNTFET types commonly recognized in the literature such as Schottky Barrier CNTFETs, Tunnel CNTFETs, and MOSFET-like CNTFETs along with their structural configurations and fabrication principles. This taxonomy and review of performance metrics aimed to provide a clear foundation for appreciating how CNTFETs address scaling limitations and could enable next generation nanoelectronics devices. By integrating insights across transistor technologies and emerging nanoscale devices, the chapter offers a solid conceptual framework essential for advancing research in CNTFET-based electronics. This sets the stage for further theoretical modeling and experimental validation, which will be addressed in subsequent parts of this thesis.

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III. Introduction

Graphene, a monolayer of carbon atoms arranged in a hexagonal lattice, is heralded as a groundbreaking material in the realm of electronics and optoelectronics. Its unique properties stem from its two-dimensional (2D) structure, which not only contributes to its strength but alsosignificantly influences its electrical characteristics. One of the most remarkable features of graphene is its exceptional electrical conductivity, attributed to the presence of π-bonds that allow for high electron mobility. This means that electrons can move through graphene more freely than they can in conventional semiconductor materials, resulting in superior performance in electronic applications. In the context of field-effect transistors (FETs), graphene serves as an ideal conductive channel. Unlike traditional semiconductor materials such as silicon, which can be limited by their intrinsic charge carrier mobility, graphene boasts charge mobility values that can exceed 20,000 $cm^2/V{\cdot}s$ under optimal conditions [1-3]. This high mobility not only enables quicker response times in electronic circuits but also supports the development of high-frequency and high-speed devices. Moreover, graphene's physical properties provide additional advantages for FET.[4] Additionally, graphene exhibits a linear energy band structure near the Dirac point, which allows for a high on/off current ratio, making it suitable for analog and digital applications alike. Graphene is also noteworthy for its thermal conductivity, which is among the highest of any known material. This characteristic is advantageous in managing heat generation in electronic devices, further contributing to their reliability and performance [5]. The combination of high charge mobility, excellent thermal properties, and a versatile platform for integration with other materials positions graphene as a frontrunner in the next generation of electronic and optoelectronic devices [6,7].

Due to its nearly negligible effective mass, graphene exhibits strong carrier mobility, significant current density, high saturation velocity, and high cut off frequency, which are all measured in units of $2.75.10^5$ cm^2/V^{-s}, 2×10^8 A/cm^2, 5.5×10^7 cm/s, and 100 GHz, respectively [8]. This substance has a zero-band gap. Although, when it is at the nanometric scale, lateral quantum confinement causes a band gap to open-up. Graphene Nanoribbons, which are thin graphene stripes with a width of less than 100 nm, have limited energy [9,10]. The outstanding current carrying capacity of GNRs is higher than 10^8 A/cm^2 for widths as small as 16 nm. The breakdown voltage (BV) is also predicted to be 2.5 V for GNRs that are 22 nm broad [11-14]. GNRs are utilized as channel material in transistors. Graphene nano ribbon field effect transistors (GNRFETs) are GNR-based transistors that are experimentally and conceptually viable alternatives to CMOS devices [15].

Two-dimensional (2D) materials have attracted significant attention for gas sensing applications due to their atomic thickness, high surface-to-volume ratio, and tunable electronic properties, which enable enhanced sensitivity and fast response times at room temperature[16-17], encompassing graphene, black phosphorus, transition metal chalcogenides (TMCs), and layered metal oxides [18],transition metal dichalcogenides (TMDs) such as MoS_2 and WS_2 have demonstrated remarkable gas sensing performance, especially when functionalized with catalytic nanoparticles or combined in heterostructures that improve charge transfer and selectivity [16-19]. For example, Pt-functionalized MoS_2 sensors have achieved sub-ppm detection limits for ammonia (NH_3) with rapid response and recovery, illustrating the potential of surface functionalization strategies [16].

Similarly, MXenes 2D transition metal carbides and nitrides have emerged as promising candidates for gas sensors due to their metallic conductivity, hydrophilic surfaces, and rich surface chemistry. $Ti_3C_2T_x$ MXene composites with conductive polymers such as polyaniline (PANI) have demonstrated ultralow detection limits and excellent cycling stability for toxic gases like NO_2, highlighting their potential for practical applications [19]. The ability to tune surface terminations in MXenes further enhances their selectivity and sensitivity.

Despite these advances, challenges remain in balancing sensitivity, selectivity, and long-term stability, particularly as many 2D sensors rely on chemical functionalization that may degrade over time [17]. In contrast, graphene nanoribbon field-effect transistors (GNRFETs) offer intrinsic advantages by leveraging electrostatic gating and quantum confinement effects, enabling highly tunable and reproducible sensing responses without extensive surface modification [16,17]. The gate-controlled modulation of carrier density in GNR channels allows dynamic adjustment of electronic properties in response to gas adsorption, providing an alternative pathway to enhance selectivity and sensitivity.

This chapter aims to provide a comprehensive and in-depth analysis of Graphene Nanoribbon Field-Effect Transistors (GNRFETs), focusing on their diverse types and architectural designs. The discussion will begin with elucidating the fundamental operating principles of GNRFETs, emphasizing the critical role of bandgap engineering in graphene nanoribbons. Following this, an overview of various fabrication techniques will be presented, highlighting how these methods influence device architectures. A systematic classification of GNRFET types including single-gate, double-gate, top-gate, and more advanced configurations will be established, detailing their structural features, operational mechanisms, and performance

characteristics. Through comparative analysis, the chapter will explore the advantages, limitations, fabrication challenges, and application-specific suitability of each architecture. Finally, the chapter will review recent scientific advancements and emerging trends, while identify ongoing challenges and project future research directions for GNRFET technology. By addressing these objectives, this chapter provides a robust academic foundation for understanding the intricate relationship between graphene nanoribbon properties, device architecture, and overall transistor performance, thereby contributing to the advancement of next generation nanoelectronics devices.

III.1 Importance of GNRFETs in Nanoelectronics

The relentless pursuit of miniaturization and enhanced performance in the semiconductor industry, encapsulated by Moore's Law, has pushed silicon-based complementary metal oxide-semiconductor (CMOS) technology to its fundamental physical and economic limits. As device dimensions approach the atomic scale, challenges such as short-channel effects, increased power dissipation, and quantum tunneling become increasingly pronounced. In this context, GNRFETs present a compelling alternative, leveraging the intrinsic advantages of graphene while addressing its bandgap deficiency.

Integrating the high carrier mobility of graphene with the engineered bandgap of GNRs, GNRFETs offer the potential for superior device characteristics, including higher operating frequencies, lower power consumption, and enhanced scalability beyond the capabilities of conventional silicon devices [20]. Their potential to overcome the limitations of silicon technology positions GNRFETs as a cornerstone for future nanoelectronic systems, ranging from ultra-fast digital circuits to highly sensitive sensors and advanced memory applications.

III.2 Fundamentals of GNRFETs

III.2.1 Basic Operating Principles of Field-Effect Transistors

Field-Effect Transistors (FETs) are fundamental semiconductor devices that control the flow of current through a channel by applying an electric field perpendicular to the channel. A typical FET comprises three terminals: the source, the drain, and the gate. The source and drain are connected to the ends of the semiconductor channel, while the gate electrode is capacitively coupled to the channel, usually separated by a thin dielectric layer. The voltage applied to the gate modulates the charge carrier concentration within the channel, thereby controlling its conductivity and, consequently, the current flowing between the source and drain. This electrostatic control allows the FET to function as an electronic switch or an amplifier. In the

'ON' state, a sufficient gate voltage induces a conductive channel, allowing current to flow. In the 'OFF' state, the gate voltage depletes the channel of carriers, effectively blocking current flow. The efficiency of this switching action is characterized by parameters such as the ON/OFF current ratio, subthreshold swing (SS), and transconductance.

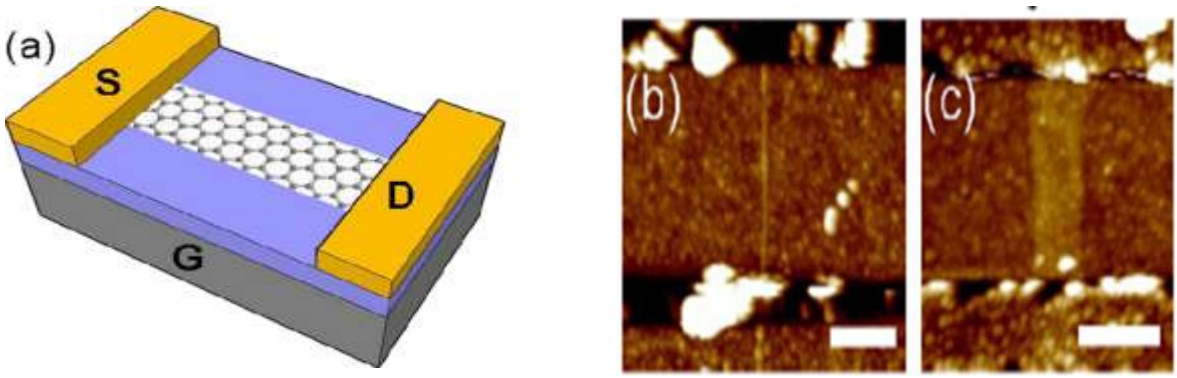

Figure III.1 *Displays images of graphene nanoribbon field-effect transistor (GNRFET) devices. (a) Diagram showing GNRFETs structure, (b) Atomic force microscopy (AFM) image of a GNRFET featuring a graphene nanoribbon approximately 2 ± 0.5 nm wide and a channel length of 236 nm. The scale bar indicates 100 nm. (c) AFM image of a wider graphene nanoribbon device with dimensions around 60 ± 5 nm in width and 190 nm in length. The scale bar corresponds to 100 nm [21].*

III.2.2 Unique Properties of Graphene Nanoribbons for FET Applications

Graphene, in its pristine, infinite sheet form, is a zero-bandgap semimetal, meaning it lacks the intrinsic bandgap necessary for efficient ON/OFF switching in digital transistors. This fundamental limitation is overcome in GNRs due to quantum confinement effects. When graphene is confined to nanoscale widths, the continuous electronic band structure of 2D graphene breaks down into discrete subbands, leading to the opening of a tunable bandgap [22]. The magnitude of this bandgap is inversely proportional to the GNR's width, with narrower ribbons exhibiting larger bandgaps. Furthermore, the electronic properties of GNRs are highly sensitive to their edge chirality (armchair or zigzag) and edge termination, allowing for precise engineering of their semiconducting behavior [23]. This ability to engineer a bandgap, combined with graphene's inherent high carrier mobility,

makes GNRs uniquely suited as channel materials for high-performance FETs, offering a pathway to devices that can operate at high frequencies with low power consumption.

III.2.3 Effect of GNR Bandgap Engineering on Transistor Behavior

The presence and tunability of a bandgap in GNRs are paramount for their application in FETs. In a GNRFET, the bandgap dictates the OFF-state current and the ON/OFF current ratio. A larger bandgap leads to a lower OFF-state current, as fewer carriers can be thermally excited across the bandgap, resulting in a higher ON/OFF ratio, which is crucial for digital logic applications. Conversely, a smaller bandgap might be desirable for high frequency analog applications where high transconductance is prioritized over a large ON/OFF ratio. By precisely controlling the GNR width and edge structure during fabrication, researchers can engineer the bandgap to meet specific device requirements. This bandgap engineering allows for optimization of key transistor parameters such as threshold voltage, subthreshold swing, and transconductance, enabling the design of GNRFETs tailored for various electronic functionalities, from ultra-low-power logic to high-speed radiofrequency circuits [24].

III.3 Fabrication Techniques Relevant to GNRFET Types

The successful realization of high-performance GNRFETs hinges critically on the ability to fabricate GNRs with precise control over their dimensions, edge morphology, and structural integrity. Over the past two decades, various fabrication strategies have been developed, broadly categorized into top-down and bottom-up approaches, each presenting distinct advantages and challenges in terms of precision, scalability, and integration with existing semiconductor manufacturing processes.

III.3.1 Top-Down vs. Bottom-Up Synthesis of GNRs

Top-down approaches involve patterning larger graphene sheets into narrow ribbons. These methods typically leverage established lithographic techniques used in conventional semiconductor fabrication. While offering compatibility with existing industrial infrastructure, top-down methods often struggle to achieve atomic precision, leading to issues such as edge roughness, width variations, and crystallographic defects. These imperfections can significantly degrade the electronic properties of GNRs, broadening the bandgap distribution and reducing carrier mobility, thereby limiting device performance and reproducibility [25].

Bottom-up approaches, conversely, involve the synthesis of GNRs atom by atom from molecular precursors. This strategy offers unparalleled control over the GNR's width, edge structure, and overall atomic precision. Techniques such as on-surface synthesis and solution-based synthesis have demonstrated the capability to produce GNRs with predefined armchair or zigzag edges and precise widths, leading to highly predictable electronic properties. However,

bottom-up methods typically face challenges in terms of scalability, throughput, and integration into large-scale device arrays, often requiring ultrahigh vacuum conditions or complex chemical processes [26].

III.3.2 Critical Fabrication Steps Influencing Device Architecture

The fabrication of Graphene Nanoribbon Field-Effect Transistors (GNRFETs) involves several essential steps that significantly affect the device architecture and overall performance. Regardless of the synthesis method selected, crucial fabrication stages determine the quality and functionality of the final GNRFET. **Figure III.2** presents a schematic overview of the fabrication procedure for graphene field-effect transistors, highlighting the key processes involved in their construction. •**GNR Synthesis and Transfer:** For top-down methods, the quality of the initial graphene film (e.g., exfoliated, CVD-grown) and the precision of the patterning and etching processes are paramount. For bottom-up methods, the control over molecular self-assembly and polymerization dictates the GNR quality. Subsequent transfer of GNRs onto target substrates, especially for devices requiring multiple layers or complex gating, is a delicate process that must preserve the GNR's integrity and minimize contamination [27].

• **Gate Dielectric Deposition:** The choice and deposition method of the gate dielectric material are crucial for achieving effective electrostatic control and minimizing gate leakage. High-k dielectric materials ($LaAlO_3$, HfO_2, Al_2O_3) are preferred due to their ability to provide high capacitance with a physically thicker layer, reducing tunneling currents.

Techniques like atomic layer deposition (ALD) are widely used for their conformal coating capabilities and precise thickness control, which are essential for ultra-thin dielectrics on GNRs [28].

• **Contact Formation:** Forming low resistance ohmic contacts between the metal electrodes (source and drain) and the GNR channel is vital for efficient charge injection and extraction. The work function alignment between the metal and the GNR, as well as the interface quality, significantly impact contact resistance. Strategies include using specific metals (palladium for p-type, titanium for n-type), contact doping, or optimizing annealing conditions [29].

• **Gate Electrode Fabrication:** The design and fabrication of the gate electrode (single, double, top, bottom, or multiple) directly define the device architecture. Precise alignment of the gate with the GNR channel is critical, especially for multi-gate structures, to ensure optimal electrostatic coupling and mitigate short-channel effects.

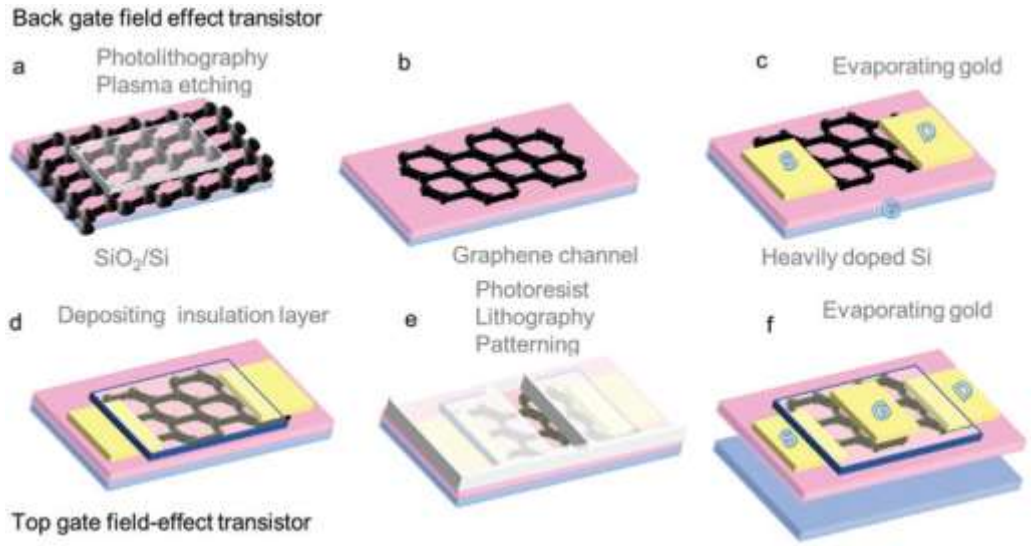

Figure III.2. *Illustrates the process for fabricating field-effect transistors (FETs) on a Si/SiO_2 substrate. Panels (a) to (c) depict the steps for creating a back-gate transistor: (a) a photomask is applied to selectively cover portions of the graphene film; (b) photolithography or plasma etching is employed to define the graphene channel; (c) gold (Au) is deposited to establish the source and drain electrodes. Panels (d) to (f) show the fabrication of a top-gate transistor: (d) deposition of Au source and drain contacts along with an insulating layer; (e) deposition of photoresist followed by photolithographic patterning; (f) Au deposition to form the top gate electrode [30].*

III.3.3 Challenges in Fabricating Different GNRFET Types

The complexity of fabrication varies significantly among different GNRFET types:

• **Single-Gate GNRFETs:** These are the simplest to fabricate, often utilizing a back-gate configuration on a silicon/silicon dioxide substrate. The main challenges lie in achieving high-quality GNRs and reliable contacts. Top-gated single-GNRFETs require additional steps for top-gate dielectric and electrode deposition, demanding precise alignment.

• **Double-Gate GNRFETs:** The dual-gate architecture, while offering superior electrostatic control, introduces significant fabrication complexities. Precisely aligning the top and bottom gates with the GNR channel and depositing high-quality dielectrics on both sides without damaging the GNR, are major hurdles. This often necessitates advanced lithography and self-alignment techniques [31].

• **Other Complex Architectures (FinFET-like, Multiple-Gate):** These advanced designs, aimed at further enhancing gate control and mitigating short-channel effects, present even greater fabrication challenges. Creating three-dimensional GNR structures or wrapping gates around

GNRs requires sophisticated patterning, etching, and deposition techniques, often pushing the limits of current nanofabrication capabilities.

The integration of novel materials, such as ferroelectrics for non-volatile memory GNRFETs, adds another layer of complexity in material compatibility and processing [32].

Overcoming these fabrication challenges is crucial for translating the theoretical advantages of various GNRFET architectures into practical, high-performance electronic devices. Continuous innovation in nanofabrication techniques, coupled with a deeper understanding of GNR material science, is essential for the future development and deployment of GNRFET technology.

III.4 Types of Graphene Nanoribbon Field-Effect Transistors

Figure III.3 illustrates the basic structure of a graphene nanoribbon field-effect transistor (GNRFET). The schematic highlights the graphene nanoribbon channel, which serves as the conducting pathway between source and drain electrodes. The gate electrode, positioned relative to the channel, modulates the electrical conductivity by controlling the carrier concentration within the nanoribbon. This structural configuration enables the unique electronic properties of GNR-based transistors, which are promising for nanoscale device applications due to their tunable bandgap and excellent carrier mobility.

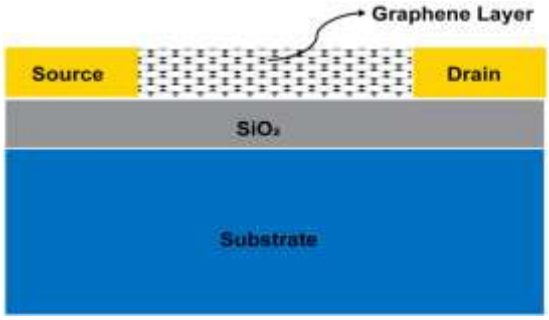

Figure III.3. *Structure of GNRFET [33]*

The principal types can be categorized as follows:

III.4.1 Schottky Barrier Graphene Nanoribbon Field-Effect Transistor (SB-GNRFET)

Schottky barrier graphene nanoribbon field-effect transistors (SB-GNRFETs) constitute a crucial subclass of GNRFET devices characterized by the formation of a Schottky barrier at the interface between the metallic contacts and the graphene nanoribbon channel. The charge carrier injection in these transistors is primarily governed by tunneling and thermionic emission mechanisms across this energy barrier, which strongly influences key device parameters such as

the on-current, off-current, and subthreshold slop [34,35]. The gate electric field modulates the Schottky barrier height and width, thus controlling the transparency of the contacts and enabling effective transistor switching. Recent developments in SB-GNRFET technology emphasize the use of atomically precise, bottom-up synthesized graphene nanoribbons with sub-nanometer widths combined with thin high-k dielectric layers, resulting in devices that demonstrate impressive on/off current ratios on the order of 10^5 and on-state currents exceeding 1 μA at low bias voltages [35,36]. Nevertheless, Schottky barrier-induced tunneling remains a limiting factor for device performance, underscoring the importance of contact optimization to reduce barrier resistance and improve carrier injection efficiency.

Moreover, the electronic behavior at the contact interface is sensitive to the number of graphene layers and their stacking order within the nanoribbon. For instance, trilayer graphene nanoribbons with ABA stacking exhibit semiconducting properties favorable for transistor action, whereas alternative stacking configurations yield characteristics more akin to semimetals, which are less advantageous for SB-GNRFET operation [34,37]. A three-dimensional depiction of the Schottky Barrier Graphene Nanoribbon Field-Effect Transistor (SB-GNRFET) structure is presented in **Figure III.4**, illustrating the fundamental device architecture. This visualization highlights the metal source and drain contacts flanking the graphene nanoribbon channel, where Schottky barriers form at the metal-semiconductor interfaces. The structure plays a crucial role in defining the charge carrier transport mechanism, with tunneling through these barriers governing the device's electrical behavior. Figure III.3 thus provides a comprehensive spatial understanding of the SB-GNRFET, essential for analyzing its performance characteristics and guiding optimization strategies.

In summary, SB-GNRFETs reflect a delicate balance between contact properties and intrinsic channel characteristics. Advances in controlling Schottky barrier parameters and graphene nanoribbon structural precision are pivotal to realizing high-performance nanoscale transistors suitable for future electronic applications.

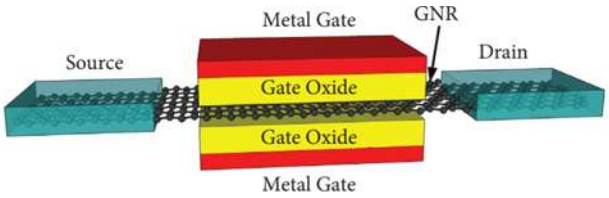

Figure III.4. *Three-dimensional representation of the Schottky Barrier Graphene Nanoribbon Field-Effect Transistor (SB-GNRFET) structure [38].*

III.4.2 Metal Oxide Semiconductor Type (MOS-GNRFET)

In MOS-GNRFETs, the source and drain reservoirs are doped with donor or acceptor impurities. Ohmic contacts are achieved by heavily doping the graphene nanoribbons in the source and drain regions, enabling the device to function similarly to a traditional MOSFET, as illustrated in **Figure.III.5.** Compared to the Schottky barrier (SB) type, the MOS configuration exhibits improved performance, including a higher on-current to off-current ratio due to the absence of ambipolar behavior, as well as enhanced transconductance. The MOS type exhibits improved saturation behavior and faster switching speeds, among other advantages. However, its fabrication is more challenging because it necessitates additional doping in the source and drain regions. When the line-edge roughness (LER) is zero, the subthreshold swing (SS) is 66.67 mV/decade, and the on/off current ratio (I_{on}/I_{off}) reaches 1.89×10^5 at a supply voltage (V_{DD}) of 0.5 V. This performance surpasses that of silicon CMOS devices, which show an SS of 93.46 mV/decade and an I_{on}/I_{off} ratio of 3.49×10^3 at $V_D = 0.7V$. However, when LER increases to 0.1, the SS degrades to 140 mV/decade, and the I_{on}/I_{off} ratio decreases to 9.8×10^1 at $V_D = 0.5V$ [39].

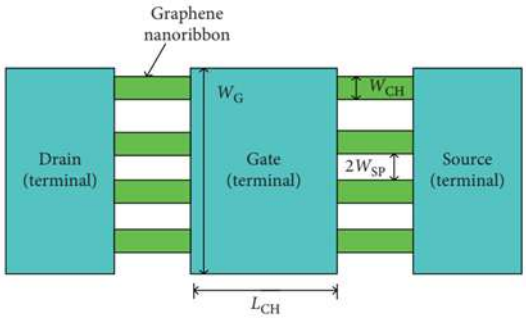

Figure III.5. *Schematic of a MOSFET-like GNRFET structure [40].*

III.5 Single-Gate GNRFETs

III.5.1 Device Structure and Gating Mechanism

Single-gate GNRFETs represent the most fundamental and historically significant architecture in the development of graphene nanoribbon transistors. In this configuration, a single gate electrode is employed to modulate the conductivity of the GNR channel. The gate can be positioned either beneath the GNR (back-gated) or on top of it (top-gated).

In a back-gated GNRFET, the GNR is typically placed directly on a dielectric layer (e.g., SiO2) grown on a highly doped silicon substrate, which serves as the global back-gate electrode. The electric field from this back-gate penetrates through the dielectric to control the carrier

concentration within the GNR. This configuration is often simpler to fabricate, making it suitable for initial fundamental studies of GNR electronic properties and device characteristics [41]. However, the relatively thick dielectric layer (typically hundreds of nanometers) associated with back-gated devices limits the electrostatic coupling efficiency, leading to higher operating voltages and reduced gate control over the channel.

Conversely, top-gated GNRFETs feature a gate electrode positioned directly above the GNR channel, separated by a thin dielectric gate. This configuration offers significantly improved electrostatic control due to the closer proximity of the gate to the channel and the possibility of using ultra-thin, high-k dielectric materials. The top-gate effectively screens the GNR from the substrate, providing more efficient modulation of the channel conductivity and enabling lower operating voltages [42].

Regardless of the gate placement, the gating mechanism in single-gate GNRFETs relies on the field-effect principle. Applying a voltage to the gate electrode creates an electric field that modulates the charge carrier density within the GNR channel. For p-type GNRFETs, a negative gate voltage accumulates holes, increasing conductivity, while for n-type GNRFETs, a positive gate voltage accumulates electrons. The presence of a bandgap in the GNR is crucial for achieving a distinct OFF-state, where the channel is depleted of carriers, leading to a low OFF-current and a high ON/OFF ratio. **Figure III.6** shows a schematic diagram of Single-Gate Graphene Nanoribbon Field-Effect Transistors (SG-GNRFETs), illustrating the basic device structure. This representation highlights the configuration where a single gate electrode modulates the conductance of the graphene nanoribbon channel, providing essential insight into the transistor's gating mechanism and electrostatic control. The schematic serves as a fundamental reference for understanding the design and operational characteristics of SG-GNRFET devices.

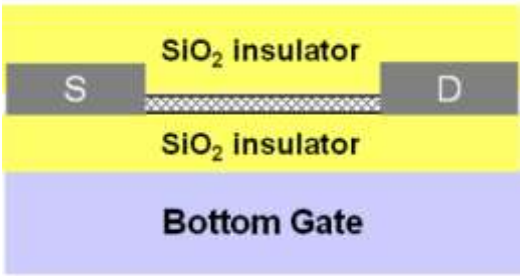

Figure III.6. *Schematic representation of Single-Gate GNRFETs [43].*

III.5.2 Advantages and Limitations

Single-gate GNRFETs offer several advantages, particularly in terms of fabrication simplicity and their utility for fundamental research:

- **Simplicity of Fabrication:**
  Especially for back-gated configurations, the fabrication process is relatively straightforward, often involving mechanical exfoliation or CVD growth of graphene, followed by lithographic patterning of GNRs and deposition of metal contacts. This simplicity has facilitated rapid prototyping and characterization in early research stages.
- **Platform for Fundamental Studies:**
  Single-gate devices have served as invaluable platforms for investigating the intrinsic electronic properties of GNRs, including bandgap opening, quantum transport phenomena, and the effects of edge disorder and defects on carrier mobility.

However, single-gate GNRFETs also suffer from significant limitations, particularly as device dimensions are scaled down:

- **Limited Electrostatic Control:**
  The single gate provides less effective control over the entire GNR channel, especially in longer channels or when using thicker gate dielectrics. This can lead to suboptimal ON/OFF ratios and higher leakage currents.
- **Susceptibility to Short-Channel Effects (SCEs):**
  As the channel length decreases, single-gate GNRFETs become highly susceptible to SCEs such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off. These effects degrade device performance, increase power consumption, and limit scalability [44].
- **Ambipolar Conduction:**
  Graphene's symmetric band structure around the Dirac point often leads to ambipolar conduction, where the device conducts both electrons and holes. While strategies like asymmetric doping or work function engineering can mitigate this, single-gate GNRFETs can still exhibit significant ambipolarity, which is undesirable for digital logic applications requiring unipolar operation.
- **Sensitivity to Substrate and Interface Traps:**

The performance of single-gate GNRFETs, particularly back-gated ones, can be significantly influenced by charge traps at the GNR-dielectric interface or within the substrate, leading to hysteresis and instability in device characteristics.

III.5.3 Typical Performance Characteristics

The performance characteristics of single-gate GNRFETs vary widely depending on the GNR quality, width, edge morphology, and fabrication techniques. Early devices often exhibited modest ON/OFF ratios (e.g., 10-100) and relatively low ON-currents, primarily due to challenges in achieving atomically precise GNRs and low-resistance contacts.

With advancements in bottom-up synthesis and improved fabrication processes, single gate GNRFETs have demonstrated significantly enhanced performance. Devices with atomically precise GNRs have shown ON/OFF ratios exceeding 10^4 at room temperature, and transconductance values comparable to or even surpassing those of silicon MOSFETs at similar dimensions [45]. However, achieving simultaneously high ON-currents, large ON/OFF ratios, and low subthreshold swings remains a challenge, often requiring trade-offs between these parameters. The inherent limitations of single-gate control, particularly in mitigating SCEs, often restrict their ultimate performance and scalability for advanced digital logic applications, paving the way for more sophisticated multi-gate architectures.

III.6 Double-Gate GNRFETs

III.6.1 Structural Design and Gate Configuration

Double-Gate GNRFETs (DG-GNRFETs) represent a significant architectural advancement over their single-gate counterparts, drawing inspiration from the successful implementation of multi-gate structures in silicon-based FinFETs. **Figure III.7** presents a schematic diagram of Double-Gate Graphene Nanoribbon Field-Effect Transistors (DG-GNRFETs), illustrating the device design where two gate electrodes symmetrically surround the graphene nanoribbon channel. This dual-gate configuration significantly improves electrostatic control over the channel, resulting in enhanced device performance compared to single-gate designs. In a DG-GNRFET, the graphene nanoribbon channel is influenced by two independent or coupled gate electrodes, typically located above and below the nanoribbon, thereby maximizing the gate's capacitive effect on charge carriers within the channel.

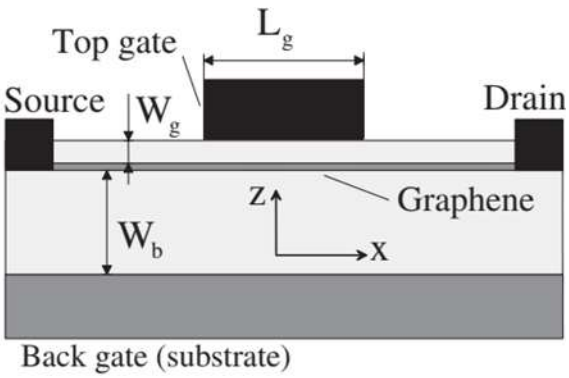

Figure III.7. *Schematic representation of Double-Gate GNRFETs [46].*

The structural design often involves sandwiching the GNR between two layers of gate dielectric, with a gate electrode on either side. For instance, a common configuration involves a bottom gate electrode on a substrate, followed by a dielectric layer, the GNR, another dielectric layer, and finally the top gate electrode [47]. The two gates can be independently biased (independent double-gate) or tied together (common double-gate). The common double-gate configuration is simpler to implement and provides enhanced gate control, while independent double-gate operation offers additional flexibility for threshold voltage tuning and ambipolarity control.

III.6.2 Electrostatic advantages: (enhanced gate control and reduced short-channel effects)

The primary motivation for adopting the double-gate architecture in GNRFETs is to significantly enhance electrostatic control over the channel, which directly translates into superior device performance, particularly at aggressively scaled dimensions. The key electrostatic advantages include:

- **Superior Gate Control:**
  With two gates influencing the channel, the electric field lines from the gate electrodes more effectively penetrate and modulate the entire volume of the GNR. This leads to a stronger coupling between the gate voltage and the channel charge, resulting in a more efficient switching action and lower operating voltages [48].
- **Reduced Short-Channel Effects (SCEs):**
  One of the most critical benefits of DG-GNRFETs is their inherent robustness against SCEs. The dual-gate configuration provides excellent screening of the channel from the drain electric field, effectively mitigating phenomena such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off. This allows for significant scaling of the channel

length without severe degradation in device performance, which is crucial for continued miniaturization in nanoelectronics [49].

- **Steeper Subthreshold Swing (SS):**
  The enhanced gate control in DG-GNRFETs leads to a sharper transition from the OFF-state to the ON-state, characterized by a steeper subthreshold swing. A lower SS is highly desirable for reducing static power consumption in digital circuits, as it allows for a lower supply voltage while maintaining a high ON/OFF ratio.
- **Higher ON/OFF Ratio:**
  By providing more effective depletion of carriers in the OFF-state and accumulation in the ON-state, DG-GNRFETs can achieve significantly higher ON/OFF current ratios compared to single-gate devices. This is essential for robust digital switching and logic applications.
- **Improved Immunity to Process Variations:**
  The dual-gate structure can also offer better immunity to variations in GNR width, dielectric thickness, and other manufacturing tolerances, leading to more uniform and predictable device characteristics across a wafer.

III.6.3 Experimental and Theoretical Performance Benchmarks

Both experimental demonstrations and theoretical simulations have consistently shown that DG-GNRFETs outperform single-gate GNRFETs in various key metrics.

Theoretical studies often predict ideal performance characteristics, serving as benchmarks for experimentalists. For instance, simulations have shown that DG-GNRFETs can achieve subthreshold swings approaching the theoretical limit of 60 mV/decade at room temperature, along with ON/OFF ratios exceeding 10^5 to 10^6, even at channel lengths below 10 nm [50]. These models also highlight the importance of precise GNR width and edge control, as well as the use of high-k gate dielectrics, for optimizing performance.

Experimental results, while often lagging behind theoretical predictions due to fabrication challenges, have made significant strides. Researchers have successfully fabricated DGGNRFETs demonstrating improved gate control, reduced ambipolarity, and enhanced ON/OFF ratios compared to single-gate devices. For example, devices with atomically precise GNRs fabricated via bottom-up methods have shown ON/OFF ratios in the range of 10^4 to 10^5, along with transconductance values indicative of high-speed operation [51]. The challenge remains in achieving wafer-scale fabrication of such high-performance devices with high yield and reproducibility.

III.6.4 Comparison with Single-Gate Counterparts

The advantages of DG-GNRFETs over single-gate GNRFETs are summarized in **Table *III.1*.** The enhanced electrostatic control provided by the dual-gate configuration directly addresses many of the limitations inherent in single-gate designs, particularly concerning scalability and power efficiency.

Table III.1. *Comparative analysis of Single-Gate vs. Double-Gate GNRFETs.*

Feature / Metric	Single-Gate GNRFETs	Double-Gate GNRFETs
ElectrostaticControl	Limited, especially for longer channels	Excellent, controls entire channel volume
Short-ChannelEffects	Highly susceptible (DIBL, Vt roll-off)	Significantly suppressed
SubthresholdSwing	Typically higher, limits power efficiency	Steeper, closer to ideal 60 mV/decade
ON/OFF Ratio	Moderate to good	High to very high
Scalability	Limited by SCEs	Enhanced, enables aggressive scaling
FabricationComplexity	Simpler	More complex, requires precise alignment and layering
PowerConsumption	Higher static power due to leakage	Lower static power due to reduced leakage

In conclusion, while the fabrication of DG-GNRFETs is more complex, their superior electrostatic control and performance characteristics make them a highly promising architecture for future high-performance and low-power nanoelectronics applications, particularly as device dimensions continue to shrink. The ongoing advancements in nanofabrication techniques are steadily bridging the gap between theoretical predictions and experimental realizations, paving the way for the practical deployment of these advanced GNRFET structures.

III.7 Top-Gate GNRFETs

III.7.1 Fabrication Approach and Gate Dielectric Integration

Top-gate GNRFETs are a crucial device architecture for achieving high-performance and scalable graphene nanoribbon transistors. Unlike back-gated devices where the gate is located beneath the substrate, top-gate configurations place the gate electrode directly on top of the GNR channel, separated by a thin dielectric layer. This proximity allows for superior electrostatic

control and is more compatible with conventional semiconductor manufacturing processes for integrated circuits.

Figure III.8 illustrates the typical fabrication process of top-gate graphene nanoribbon field-effect transistors (GNRFETs), which involves several essential steps. First, the GNRs are synthesized (either top-down or bottom-up) and transferred onto a substrate with prepatterned source and drain contacts. Following this, a high-quality gate dielectric layer is deposited directly onto the GNRs. This step is critical, as the dielectric must be ultra-thin, uniform, and free of defects to ensure efficient gate coupling and minimal leakage current. Atomic Layer Deposition (ALD) is the preferred technique for gate dielectric integration due to its ability to deposit conformal and pinhole-free films with precise thickness control at relatively low temperatures, which is crucial for preserving the integrity of the GNRs [52]. Common high-k dielectric materials used include HfO_2, Al_2O_3, and ZrO_2. Finally, the top gate electrode (e.g., metal or doped polysilicon) is deposited and patterned on top of the dielectric layer, completing the device structure.

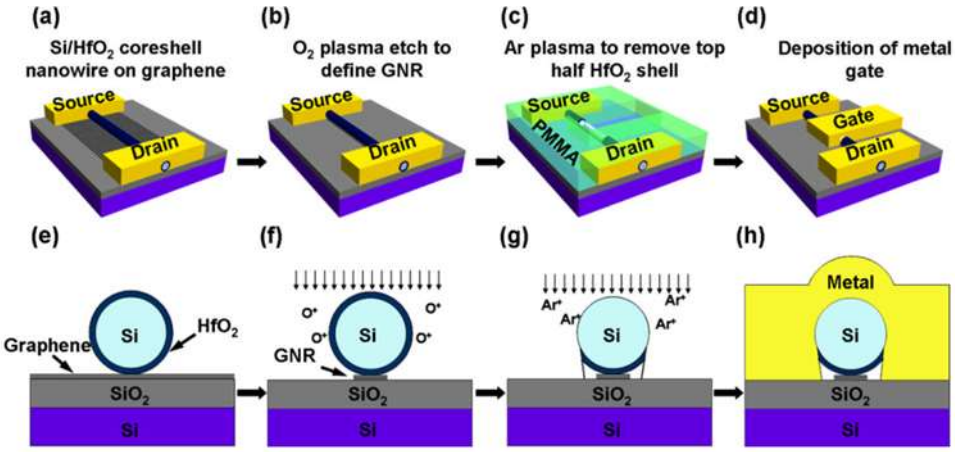

Figure III.8. *Schematic representation of the fabrication process for top-gated graphene transistors utilizing Si/HfO_2 core-shell nanowires as both the etching mask and top gate.* ***(a)*** *and* ***(e)*** *show the alignment of a Si/HfO_2 core-shell nanowire onto the graphene surface through a dry-transfer method, followed by the fabrication of source-drain electrodes via electron-beam lithography.* ***(b)*** *and* ***(f)*** *depict the removal of unprotected graphene using oxygen plasma etching, leaving only the graphene nanoribbon (GNR) beneath the nanowire, which remains connected to two large graphene regions under the source and drain electrodes.* ***(c)*** *and* ***(g)*** *illustrate the selective etching of the top half of the HfO_2 shell with argon plasma to expose the silicon core gate for external electrode contact. Finally,* ***(d)*** *and* ***(h)*** *present the definition of the top gate electrode through lithography and metallization processes.[53]*

III.7.2 Benefits of Top-Gate Configuration on Device Scalability and Switching Performance

The top-gate configuration offers significant advantages that directly impact the scalability and switching performance of GNRFETs:

• Enhanced Electrostatic Control:

The close proximity of the top-gate to the GNR channel provides strong electrostatic coupling, allowing for efficient modulation of the channel conductivity with lower gate voltages. This leads to improved transconductance and higher ON-currents [54].

• Reduced Short-Channel Effects:

By effectively screening the GNR channel from the influence of the drain electric field, top-gates help mitigate short-channel effects such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off. This is particularly important for scaling down the channel length to achieve higher device densities and operating frequencies.

• Improved ON/OFF Ratio and Subthreshold Swing:

The superior gate control enables a more effective depletion of carriers in the OFF-state and accumulation in the ON-state, resulting in higher ON/OFF current ratios and steeper subthreshold swings. A low subthreshold swing is essential for low-power applications, as it allows for a sharp transition between the ON and OFF states with minimal voltage swing.

• Compatibility with CMOS Technology:

The top-gate architecture is more akin to the gate-all-around (GAA) or FinFET structures used in advanced silicon CMOS technology, making GNRFETs with top-gates more amenable to integration into existing semiconductor fabrication lines. This compatibility is vital for the eventual commercialization of GNRFETs.

III.7.3 Use of High-k Dielectrics and Impact on Electrical Characteristics

The integration of high-k dielectric materials is indispensable for optimizing the electrical characteristics of top-gate GNRFETs. High-k dielectrics possess a higher dielectric constant (κ) compared to traditional SiO_2, allowing for a larger gate capacitance (C_g) for a given physical thickness. This translates to several critical benefits:

• Increased Gate Capacitance:

A higher C_g leads to stronger gate control over the channel, improving the transconductance (g_m) and enabling higher drive currents. This is particularly important for GNRFETs, where the channel is atomically thin and requires efficient electrostatic modulation.

• Reduced Gate Leakage Current:

By allowing for a physically thicker dielectric layer while maintaining high capacitance, high-k materials effectively reduce direct tunneling leakage current through the gate dielectric. This is crucial for minimizing static power consumption and improving device reliability [55].

• Lower Operating Voltage:

The enhanced gate coupling facilitated by high-k dielectrics allows the device to operate effectively at lower supply voltages, further contributing to reduced power consumption, which is a key requirement for portable and energy efficient electronics.

• Improved Subthreshold Swing:

The stronger gate control also contributes to a steeper subthreshold swing, leading to a more abrupt switching behavior and better power efficiency.

However, the integration of high-k dielectrics with GNRs also presents challenges, such as ensuring a clean and defect-free interface to minimize charge trapping and mobility degradation. Surface functionalization or buffer layers are sometimes employed to improve the interface quality and enhance device performance. Despite these challenges, the benefits offered by high-k dielectrics are paramount for realizing high-performance and energy-efficient top-gate GNRFETs.

III.8 Other GNRFET Variants

Beyond the widely studied single-gate, double-gate, and top-gate configurations, the versatility of graphene nanoribbons has inspired the exploration of numerous other GNRFET architectures. These variants often aim to address specific performance bottlenecks, enable novel functionalities, or improve compatibility with emerging technologies.

III.8.1 Back-Gated and Bottom-Gated Devices

While briefly mentioned in the context of single-gate GNRFETs, it is important to distinguish and elaborate on back-gated and bottom-gated devices.

Back-gated GNRFETs typically utilize a heavily doped silicon substrate as the global back gate electrode, with a thermally grown silicon dioxide (SiO_2) layer serving as the gate dielectric. This

configuration is often the simplest to fabricate, making it a common choice for initial material characterization and fundamental studies of GNR properties [56]. The main advantages include ease of fabrication and the ability to study GNRs without complex top-gate processing. However, their limitations include poor electrostatic control due to the relatively thick SiO_2 dielectric, high operating voltages, and susceptibility to substrate induced scattering and charge traps, which can lead to hysteresis and degraded performance.

Bottom-gated GNRFETs are a more specific subset where a patterned gate electrode is fabricated on the substrate before the GNR is transferred or grown. This allows for localized gate control, unlike the global control of a back-gate. While still simpler than top-gated or double-gated structures, they share some of the limitations of back-gated devices regarding gate coupling efficiency if the dielectric is thick. However, they offer better control over individual devices compared to a global back-gate.

III.8.2 Multiple-Gate Configurations (e.g., Tri-Gate, Surrounding Gate)

Inspired by the success of multi-gate architectures in silicon technology (e.g., Fin FETs), researchers have extended these concepts to GNRFETs to further enhance electrostatic control and mitigate short-channel effects.

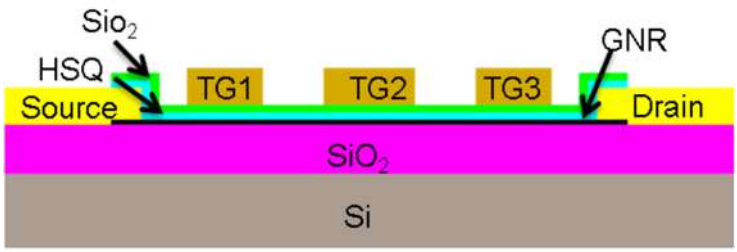

Figure III.9. *Cross-sectional schematic illustration of the triple top-gate transistor [58].*

Tri-gate GNRFETs involve a GNR channel with gate electrodes on three sides, typically a top gate and two side gates. This configuration provides improved gate control compared to double-gate structures, leading to better suppression of short-channel effects, steeper subthreshold slopes, and higher ON/OFF ratios [57]. The fabrication complexity increases significantly due to the need for precise patterning and dielectric deposition around the GNR on multiple facets.

Surrounding-gate (or Gate-All-Around, GAA) GNRFETs represent the ultimate in electrostatic control, where the gate electrode completely encircles the GNR channel. This

architecture offers the most effective control over the channel, virtually eliminating short channel effects and providing near-ideal subthreshold characteristics. GAA GNRFETs are highly promising for ultimate scaling and ultra-low-power applications [59]. However, their fabrication is exceedingly challenging, often requiring sophisticated self-assembly techniques or advanced etching processes to create the wrapped gate structure around the nanoscale GNR. **Figure III.8** provides a cross-sectional schematic illustration of a triple top-gate transistor, showcasing the layered architecture and gate electrode arrangement. This detailed visualization highlights how the three top gates are strategically positioned to modulate the channel beneath them, offering enhanced electrostatic control and improved device performance. The schematic serves as an important reference for understanding the structural design and operational advantages of triple top-gate transistor configurations.

III.8.3 Novel Architectures (Non-volatile memory GNRFETs using ferroelectric gates)

Beyond traditional switching applications, GNRFETs are being explored for novel functionalities, such as non-volatile memory. Ferroelectric GNRFETs integrate a ferroelectric material as the gate dielectric. Ferroelectric materials exhibit a spontaneous and reversible electric polarization that can be switched by an external electric field. This polarization can be used to modulate the threshold voltage of the GNRFET, allowing for two stable resistance states (ON and OFF) even after the gate voltage is removed, thus enabling non-volatile memory operation [60].

A schematic representation (**Figure III.10**) illustrating the final geometry of a graphene-based ferroelectric memory device provides a clear visualization of its structural components and layout. This diagram is essential for understanding how the ferroelectric layer interacts with the graphene channel to enable memory functionalities, emphasizing the critical design aspects that influence device performance and reliability. These devices offer the potential for high-density, low power, and fast non-volatile memory, leveraging the excellent switching properties of GNRs and the memory capabilities of ferroelectrics. Challenges include material compatibility, interface quality, and endurance of the ferroelectric layer.

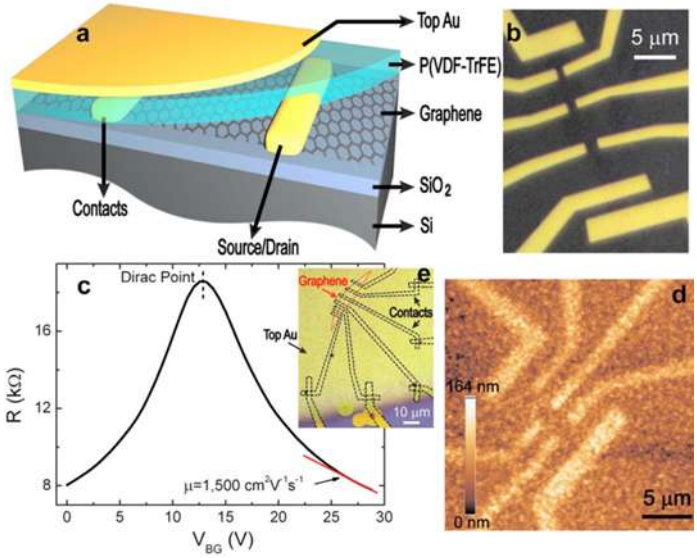

Figure III.10. *(a) Schematic representation of the final geometry of a graphene-based ferroelectric memory device. (b) Optical micrograph of a graphene sample configured in a Hall bar geometry, depicting the arrangement of the bottom electrodes. (c) Resistance (R) versus back-gate voltage (V_{bg}) characteristics of the graphene sample measured in a two-terminal setup prior to coating with the ferroelectric polymer P(VDF-TrFE). (d) Atomic force microscopy (AFM) image of a different graphene sample following spin coating with P(VDF-TrFE); the observed contrast arises from the distinct crystallization behavior of the P(VDF-TrFE) polymer on SiO_2, graphene, and gold electrodes, respectively. (e) Optical micrograph of the fully fabricated device.[61]*

III.8.4 Network-Based GNRFETs Using GNR Films or Ribbon Networks

While most GNRFET research focuses on individual GNRs, the concept of network-based GNRFETs explores the use of films or networks composed of multiple interconnected GNRs. This approach aims to overcome the challenges associated with fabricating and integrating individual, atomically precise GNRs into large-scale circuits. By forming a random or aligned network of GNRs, it becomes possible to create larger-area devices that are more amenable to scalable fabrication techniques like solution processing or chemical vapor deposition [62].

In these devices, the overall conductivity of the network is modulated by the gate electrode. While individual GNRs in the network may not have perfectly controlled properties, the collective behavior of the network can still exhibit semiconducting characteristics. The performance of network-based GNRFETs, such as ON/OFF ratio and mobility, depends on factors like GNR density, connectivity, and the quality of inter-ribbon junctions. While they may not achieve the ultimate performance of single, atomically precise GNRFETs, network based devices offer a pathway towards more practical and scalable GNR-based electronics for

applications where high performance can be traded for ease of fabrication and cost effectiveness, such as flexible electronics or large-area sensors.

Figure III.11 (a) depicts a schematic diagram of a graphene nanoribbon (GNR) network field-effect transistor (FET), with a highlighted potential percolation path shown in green. Red circles mark the locations where charge transfer occurs between closely spaced nanoribbons. The electrical current flows through the GNR channel, bridging the gold (Au) source and drain electrodes. The GNR film covers the entire substrate surface. It should be noted that the illustration is not drawn to scale. **Figure III.11 (b)** shows an optical micrograph of the GNR network FET, where the blue area represents the SiO_2 substrate and the gold regions correspond to the metallic contacts. An inset presents a scanning electron microscopy (SEM) image focused on the channel, illustrating current flow through the interconnected GNR network with Au electrodes false-colored in yellow. The channel gap measures about 600 nm. **Figure III.10(c)** displays Raman spectra of a 5-armchair graphene nanoribbon (5-AGNR) film before and after being transferred from a gold substrate onto silicon dioxide. The spectra reveal D and G peaks near 1340 cm^{-1} and 1565–1595 cm^{-1} respectively, characteristic of sp^2 carbon. A band at approximately 1220 cm^{-1} corresponds to carbon-hydrogen stretching modes along the ribbon edges, while low-frequency modes are attributed to radial breathing-like modes dependent on the ribbon width, defined by the number of carbon atoms across it.

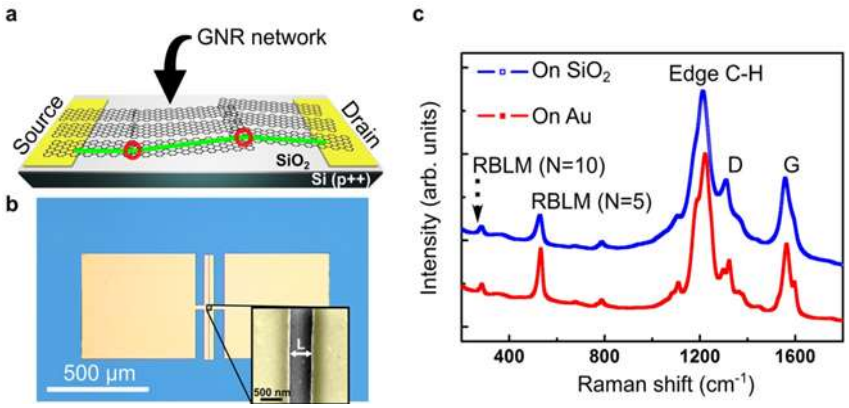

Figure III.11. *(a) Schematic illustration of a Graphene nanoribbon (GNR) network field-effect transistor (FET) Figure III-11. (b) Optical micrograph of the GNR network FET device. (c) Raman spectral of a 5-armchair graphene nanoribbon (5-aGNR) film [63].*

III.9 Discussion on Trade-Offs Between Device Complexity, Scalability, and Electrical Performance

The choice of GNRFET architecture involves a complex interplay of trade-offs among fabrication complexity, scalability, and desired electrical performance. Generally, there is a direct correlation between increased architectural complexity and enhanced electrical performance, particularly in terms of electrostatic control and short-channel effect mitigation.

III.9.1 Fabrication Complexity vs. Performance

Simpler architectures like back-gated single GNRFETs are easier to fabricate, making them ideal for initial research and proof-of-concept studies. However, their limited gate control and susceptibility to short-channel effects restrict their performance for advanced digital applications. As the architecture evolves towards double-gate, tri-gate, and surrounding-gate configurations, the fabrication complexity escalates significantly, demanding advanced lithography, precise alignment, and sophisticated material deposition techniques. This increased complexity is justified by the substantial improvements in electrostatic control, leading to higher ON/OFF ratios, steeper subthreshold swings, and better scalability, which are critical for high-performance and low-power electronics [64].

- **Scalability:**

  Scalability refers to the ability to shrink device dimensions while maintaining or improving performance. Multi-gate architectures (double-gate, tri-gate, surrounding gate) are inherently more scalable than single-gate devices due to their superior control over the channel, which effectively suppresses short-channel effects. This allows for aggressive scaling of the channel length without significant performance degradation.

However, the fabrication challenges associated with these complex 3D structures can limit their practical scalability in mass production [65].

- **Electrical Performance:**

  The ultimate goal of GNRFET design is to achieve high electrical performance, characterized by high ON-currents, low OFF-currents, steep subthreshold swings, and high operating frequencies. Double-gate and surrounding-gate GNRFETs consistently demonstrate superior electrical performance due to their enhanced electrostatic control. The ability to engineer the bandgap of GNRs through precise width and edge control further contributes to optimizing these performance metrics. However, achieving ideal

performance often requires atomically precise GNRs, which are challenging to fabricate on a large scale [66].

III.9.2 Suitability of Each Type for Different Applications

The diverse characteristics of different GNRFET types make them suitable for a variety of applications:

- **Digital Logic:**
  For high-performance and low-power digital logic circuits, Double-Gate, Tri-Gate, and Surrounding-Gate GNRFETs are the most promising due to their excellent electrostatic control, high ON/OFF ratios, and superior scalability. Their ability to mitigate short-channel effects makes them ideal for future generations of microprocessors and memory [67].
- **High-Frequency Electronics:**
  The high carrier mobility in GNRs makes all GNRFET types potentially suitable for high-frequency applications. However, Top-Gate and Double-Gate GNRFETs are particularly well-suited due to their improved gate control and reduced parasitic capacitances, enabling higher cutoff frequencies and maximum oscillation frequencies for RF circuits, mixers, and amplifiers [68].
- **Sensing Applications:**
  Single-Gate (SG), Double-Gate (DG), and Network-based Graphene Nanoribbon Field Effect Transistors (GNRFETs) are highly attractive for sensing and optoelectronic applications due to their large surface-to-volume ratio and strong sensitivity to environmental changes. These features make GNRFETs effective as biosensors, chemical sensors, and photodetectors. The tunable bandgaps of GNR channels enable wavelength selective photo detection and enhanced molecular detection sensitivity, which is particularly valuable in medical and environmental monitoring. Double-gate GNRFETs offer improved electrostatic control and reduced short channel effects, enhancing sensitivity and device performance compared to single-gate configurations. Furthermore, the simpler fabrication processes and potential for large-area integration make these devices well-suited for applications where ultra-high performance may be balanced with cost-effectiveness and manufacturing ease. These advantages position both single-gate and double-gate GNRFETs as promising candidates for next generation sensing technologies [69,70].

- **Non-Volatile Memory:**
  Ferroelectric GNRFETs are specifically designed for nonvolatile memory applications, offering the potential for high-density, low-power, and fast memory solutions by leveraging the ferroelectric switching mechanism [71].
- **Fundamental Research and Prototyping:**
  Back-gated Single-Gate GNRFETs remain invaluable for fundamental research into GNR properties and for rapid prototyping due to their relative ease of fabrication. The selection of GNRFET architecture is driven by a careful consideration of the desired application, the achievable fabrication complexity, and the required performance metrics. Continued research and development across all these architectural variants will be crucial for realizing the full potential of GNRFET technology in diverse electronic systems [72].

III.10 Recent Advances and Emerging Trends

The field of GNRFETs is rapidly evolving, driven by continuous innovations in materials science, nanofabrication, and device engineering. Recent advances are pushing the boundaries of performance, exploring new functionalities, and addressing the challenges associated with large-scale integration.

III.10.1 Latest Research Highlights in GNRFET Architectures

Recent research has focused on refining existing GNRFET architectures and proposing novel designs to further enhance performance metrics and expand their application space.

- **Enhanced Performance in Scaled Devices:**
  Significant efforts are directed towards achieving high-performance GNRFETs at aggressively scaled dimensions. This includes optimizing the design of double-gate and multi-gate GNRFETs to minimize short channel effects and improve subthreshold characteristics. For instance, studies are exploring 22 nm GNRFET designs for low-power logic applications, demonstrating improved propagation delays and power efficiency [73]. The focus is on achieving steep subthreshold swings and high ON/OFF ratios crucial for next-generation digital circuits.
- **Ternary Logic and Multi-Valued Logic Circuits:**
  A notable emerging trend is the exploration of GNRFETs for multi-valued logic (MVL) and ternary logic circuits. Unlike binary logic (0 and 1), ternary logic uses three states (0, 1, and 2), which can potentially increase information density and reduce interconnect complexity in integrated circuits.GNRFETs, with their tunable bandgaps and ambipolar

characteristics (which can be controlled), are well-suited for designing ternary inverters and logic gates [74,75].Recent works have proposed highly efficient ternary half-adders and multipliers utilizing GNRFETs, showcasing their potential for novel computing paradigms.

- **Analog Circuit Applications:**

  While much attention is given to digital applications, GNRFETs are also being investigated for analog circuit applications. Research is exploring the use of GNRFETs in operational transconductance amplifiers (OTAs) and other analog building blocks, leveraging their high transconductance and potential for high-frequency operation [76]. Performance optimization of GNRFET inverters at advanced technology nodes (e.g., 32nm) also highlights their suitability for analog signal processing.

III.10.2. Integration with Other Materials and Hybrid Devices

The integration of GNRFETs with other advanced materials and the development of hybrid devices represent a significant trend, aiming to combine the unique properties of GNRs with complementary functionalities.

- **Hybrid Fin-FET-GNRFET Designs:**

  To leverage the established fabrication infrastructure and performance benefits of silicon FinFETs, hybrid designs are being explored. These approaches combine FinFETs with GNRFETs to create novel logic circuits or memory cells. For example, hybrid adder-subtractor designs utilizing both FinFET and GNRFET technologies have been proposed, aiming to optimize performance and power consumption [77]. This integration strategy seeks to bridge the gap between current silicon technology and future graphene-based electronics.

- **GNRFETs with Phase Change Materials (RRAM):**

The integration of GNRFETs with resistive random-access memory (RRAM) is a promising area for non-volatile memory and neuromorphic computing applications. The gate-controlled graphene-based resistive random-access memory (GC-GRRAM) device is characterized by a layered structure that enables efficient memory switching. **Figure III.12(a)** illustrates the overall device architecture, highlighting the configuration that facilitates gate control over the resistive states. The cross-sectional transmission electron microscopy (TEM) image in **Figure III.12(b)** reveals the detailed Al/AlOx/graphene/SiO2 stacking sequence, demonstrating the quality and uniformity of the layers. Complementing this, the atomic force microscopy (AFM) image in **Figure III.12(c)** provides a surface topography view of the device,

showing features critical for its electrical performance. Together, these visualizations underscore the sophisticated design and fabrication precision essential for the GC-GRRAM's reliable operation. RRAM devices, which store information based on resistance changes, can be combined with GNRFETs to create compact and energy-efficient memory cells or synapses for artificial neural networks. Recent designs of multi-valued logic gates using RRAM and GNRFETs demonstrate the potential for high density and reconfigurable computing [78].

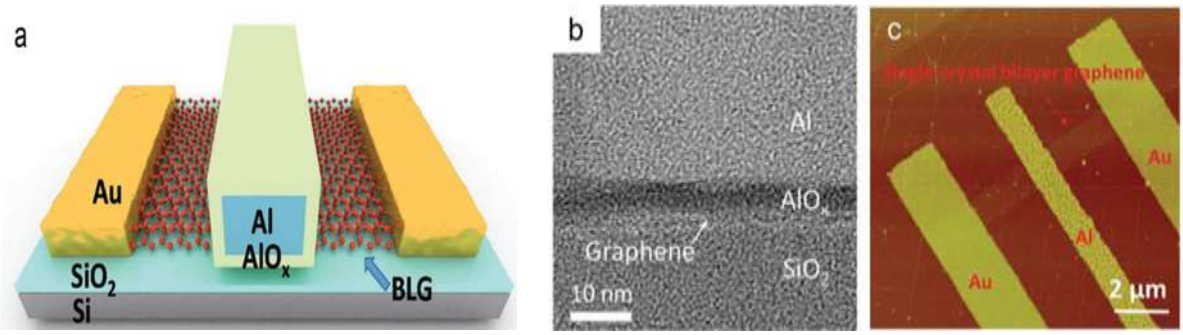

Figure III.12. (a) *Diagram illustrating the structure of the gate-controlled graphene-based resistive random-access memory (GC-GRRAM) device.* ***(b)*** *Cross-sectional transmission electron microscopy (TEM) image showcasing the Al/AlOx/graphene/SiO_2 stack. (c) Atomic force microscopy (AFM) image of the device [79].*

- **Integration with 2D Materials:**

  Beyond graphene, the vast family of two-dimensional (2D) materials (e.g., transition metal dichalcogenides like MoS_2, WS_2) offers diverse electronic and optical properties. Hybrid devices combining GNRs with other 2D materials are being investigated to create heterostructures with tailored functionalities. This could lead to novel devices with enhanced performance or multi-functional capabilities, such as photodetectors or flexible electronics [80].

- **Superconducting Hybrid Devices:**

  An emerging and highly interdisciplinary area involves merging GNRFETs with superconducting devices, such as Josephson junctions.This integration aims to create high-speed terahertz devices or quantum computing components, leveraging the unique electronic properties of graphene at low temperatures and the quantum phenomena in superconductors [81].

III.10.3 Challenges Remaining and Future Directions for Device Improvement

Despite the remarkable progress, several significant challenges must be addressed for the widespread adoption of GNRFET technology:

- **Scalable and Reproducible Fabrication:**
  The most critical challenge remains the development of scalable, cost-effective, and reproducible fabrication methods for atomically precise GNRs with high yield. While bottom-up synthesis offers precision, scaling it to wafer-level production is complex. Top-down methods struggle with edge roughness and variability. Future research needs to focus on hybrid approaches or novel techniques that combine precision with scalability [82,83].
- **Contact Resistance Reduction:**
  High contact resistance between the GNR and metal electrodes continues to be a major bottleneck, limiting the ON-current and overall device performance. Innovative contact engineering strategies, including new contact materials, doping techniques, and interface passivation, are crucial [84].
- **Variability Control:**
  Ensuring uniformity in GNR width, edge structure, and electronic properties across large device arrays is essential for reliable circuit operation. Process variations can lead to significant device-to-device variability, impacting yield and performance predictability [66].
- **Thermal Management:**
  As GNRFETs are scaled down and integrated into dense circuits, localized heating can become a significant issue, potentially degrading performance and reliability. Effective thermal management strategies, including novel heat dissipation materials and device designs, are necessary [85].
- **Reliability and Stability:**
  Long-term reliability, environmental stability, and robustness under various operating conditions need to be thoroughly investigated. This includes understanding degradation mechanisms and developing encapsulation strategies [86].

Future directions for GNRFET research will likely involve continued exploration of novel architectures, such as vertical GNRFETs or those incorporating ferroelectric materials for advanced memory. The integration of GNRFETs with other emerging materials, including

topological insulators and 2D semiconductors, will open new avenues for multi-functional devices. Furthermore, the development of advanced simulation and modeling tools will be crucial for predicting device behavior and guiding experimental efforts. Ultimately, the successful translation of GNRFET technology from laboratory to industry will depend on overcoming these challenges through interdisciplinary collaboration and sustained research investment, paving the way for a new era of high-performance and energy efficient nanoelectronics [87].

Conclusion

This chapter has undertaken a detailed and critical examination of Graphene Nanoribbon Field-Effect Transistors (GNRFETs), underscoring the paramount influence of device architecture on their operational efficacy and functional versatility. Beginning with foundational principles, we emphasized how quantum confinement within graphene nanoribbons facilitates precise bandgap engineering, thereby enabling the transition of graphene into a viable semiconducting channel for transistor applications. The synthesis of GNRs with controlled width and edge configurations via state-of-the-art bottom-up fabrication strategies has emerged as essential for tailoring electronic properties, directly impacting device behavior.

Our systematic analysis traversed a spectrum of GNRFET architectures, from single-gate designs noted for fabrication simplicity but constrained by electrostatic control and short-channel effects, to double-gate configurations exhibiting superior gate modulation, enhanced scalability, and markedly improved performance metrics including steeper subthreshold slopes and enhanced ON/OFF current ratios. Top-gate devices were highlighted for their CMOS compatibility and ability to leverage high-k dielectrics for electrical optimization. Additionally, alternative architectures such as back-gated, multi-gate (tri-gate, surrounding-gate), ferroelectric, and network-based GNRFETs were explored, each carving a niche with unique advantages tailored to specific applications or fabrication challenges.

The practical implementation of GNRFET technology is fundamentally governed by the interplay between architectural complexity, manufacturability, and electrical performance. Architectures that afford superior electrostatic integrity, such as double-gate and surrounding-gate designs, are indispensable for cutting-edge digital logic circuits and ultra-low-power electronics, where suppression of short-channel effects and maximization of ON/OFF ratios are

critical. However, the increased fabrication intricacy intrinsic to these advanced geometries imposes significant hurdles concerning scalability and cost-efficiency.

In contrast, simpler configurations like back-gated single-GNRFETs or network-based arrays, while delivering comparatively reduced peak performance, offer more straightforward, scalable, and economically viable fabrication routes, positioning them as contenders for applications tolerant to performance trade-offs, including flexible electronics and large-area sensor deployments. The advent of hybrid systems incorporating GNRFETs with complementary technologies such as Fin FETs and resistive random-access memory (RRAM) exemplifies an integrative paradigm that harnesses material and architectural synergies to realize multifunctional, high-performance electronic platforms [70,69].

The trajectory of GNRFET research is marked by vigorous innovation aimed at surmounting extant technical challenges and harnessing the full promise of graphene-based nanoelectronics. Continued refinement of synthesis methodologies is imperative to attain atomic-level precision, exceptional uniformity, and industrial-scale scalability of graphene nanoribbons. Addressing critical issues such as contact resistance, device-to-device variability, and thermal dissipation constitutes the foundation for transitioning GNRFETs from laboratory prototypes to viable commercial devices.

Future research avenues are anticipated to explore novel device architectures, including vertical GNRFETs, and the integration of GNRs with emergent quantum materials such as topological insulators, promising unprecedented device functionalities and enhanced performance benchmarks. The maturation of GNRFET technology will necessitate interdisciplinary collaboration, bridging materials science, nanofabrication technologies, device physics, and integrated circuit design. As silicon-based electronics approach fundamental scaling limits, GNRFETs offer a compelling alternative pathway toward faster, more energy-efficient, and multifunctional nanoelectronic devices aligned with evolving demands in computation, communication, and sensing domains. The architectural diversity intrinsic to GNRFETs will continue to be a decisive factor in shaping the future landscape of carbon-based electronics, with double-gate GNRFETs poised as frontrunners for advanced sensing and logic applications.

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Chapter IV

Introduction

This chapter provides an in-depth presentation of the mathematical modeling framework employed throughout this dissertation, specifically focusing on the operation of the overlapping-gate carbon nanotube field-effect transistor (OG-CNTFET). The chapter begins with a comprehensive description of the studied transistor component, establishing necessary context and foundational understanding of its structural and electronic characteristics [1,2]. Subsequently, an analytical model is developed to characterize the current-voltage (I–V) behavior under two distinct operational regimes: in darkness and under external illumination. This dual-condition approach facilitates a thorough investigation of the device's electrical response and enables precise calculation of the total charge distribution within the transistor channel, a critical factor influencing device performance [2,3].The developed model integrates advanced electrostatic considerations, notably the gate oxide capacitance, which plays a pivotal role in modulating the transistor's channel potential and overall electrostatic control [1]. The theoretical framework is formulated through an innovative synthesis and extension of existing physical models and empirical studies, capturing the unique quantum transport phenomena intrinsic to OG-CNTFETs under varying environmental stimuli, including optical excitation [2,4]. Following the model formulation, the chapter details the simulation methodology, including the computational setup, parameter selection, and calculation workflow. Numerical results are presented and interpreted with particular attention to the drain current versus bias voltage characteristics in the dark. Further, the impact of optical current on these electrical characteristics is rigorously examined, alongside a parametric study analyzing the influence of key device and environmental parameters on the optical and total drain currents, with the latter defined as the sum of the dark drain current and the photogenerated current [1,3].Through this integrative modeling and simulation approach, Chapter 4 establishes the theoretical and computational foundation essential for the subsequent experimental validation and application-oriented analysis of OG-CNTFETs within this research.

IV.1. Comprehensive Overview of the OG-CNTFET Device

The OG-CNTFET is fabricated based on a CNTFET structure featuring a p-type back gate. The gate dielectric consists of silicon oxide, formed through localized thermal oxidation (**Figure IV.1.a**), enabling the creation of a high-quality, spatially confined SiO_2 dielectric layer. A thin film of poly(3-octylthiophene) (P_3OT) is subsequently deposited over the entire wafer using a specialized deposition technique.

The thin film of poly(3-octylthiophene) (P_3OT) is applied via spin-coating, achieving an approximate thickness of 5 nm [5]. P_3OT is a photosensitive polymer commonly utilized in solar energy conversion to electricity [6,7]. Upon illumination, photo-generated electrons influence the conduction channel of the OG-CNTFET for durations exceeding one day (**Figure IV.1.b**) [5]. Consequently, this transistor functions not only as an optoelectronic device but also as a non-volatile memory element.

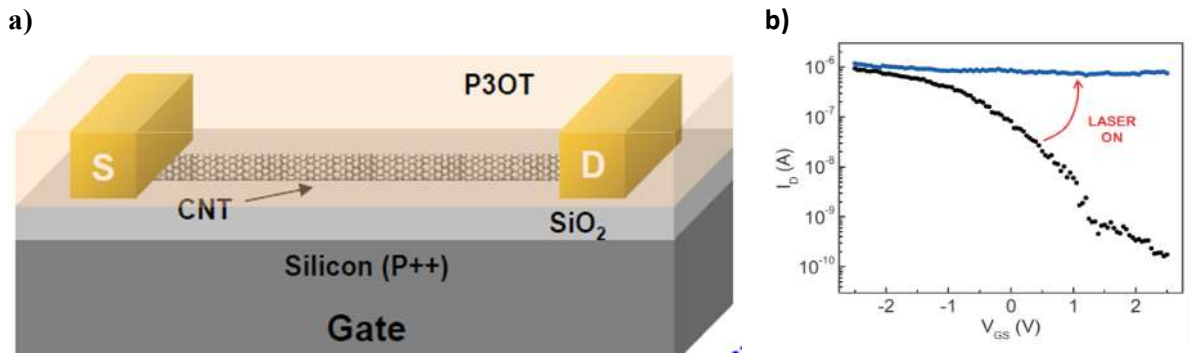


Figure* IV.*1.* *a) *Schematic representation of an OG-CNTFET.*
b) *I_{ds}-V_{gs} characteristics of an OG-CNTFET measured in the dark and under illumination [60].*

IV.2. Modeling of the Static Characteristics of the OG-CNTFET Transistor

IV.2.1. Characteristics in darkness

To calculate the I-V characteristics of CNTFETs, we based our work on the study by Dinh Sy Hien et al. [8], which presents a simple and well-explained analytical model capturing the specific physical phenomena of CNTFETs. The Landauer formalism, along with the assumption of ballistic transport valid when the channel length is shorter than the carriers' mean free path was adhered to and employed in the modeling.

The accurate calculation of subband minima, the effective number of subbands, and the drain current in CNTFETs represents the primary focus of most physical models in this field, including the present work. Additionally, our approach prioritizes models that are mathematically straightforward while providing clear explanations of the underlying physical phenomena.

a. Dispersion Relation in CNTs

In this section, the method employed is the zone folding technique to construct the band structure of the CNT. The CNT is characterized by the chiral vector C_h, and the translation vector T, which are defined as follows:

$$\overrightarrow{C_h} = n_1\overrightarrow{a_1} + n_2\overrightarrow{a_2}, \qquad 0 \leq n_2 \leq n_1 \tag{IV.1}$$

$$\vec{T} = t_1\overrightarrow{a_1} + t_2\overrightarrow{a_2}, \tag{IV.2}$$

Where : n_1, n_2, t_1 et t_2 are integers.

The chiral and translation vectors define the unit cell of the CNT, which is a cylinder with diameter dt and length | T |. The primitive unit cell aids in constructing the reciprocal lattice and the first Brillouin zone, which are crucial for determining the electronic band structure and the subband minima of the CNT.

In this case, the dispersion relation of graphene that was utilized is given by [9]:

$$E(k) = \pm\gamma\sqrt{1 + 4cos\left(\frac{a\sqrt{3}}{2}k_X\right)cos\left(\frac{a}{2}k_Y\right) + 4cos^2\left(\frac{a}{2}k_Y\right)} \tag{IV.3}$$

Where: $\gamma = 3.1eV$ and $a = 2.46A^{\circ}$.

The carbon nanotube can be viewed as a cylindrical sheet of graphene, and the wave vector (K) values are determined by the periodicity of the internal potential and the boundary conditions. The wave vector values are shown as follows:

$$K = \frac{2\pi}{C_h}q, \qquad q = 0,1,2,\ldots\ldots\ldots,N-1 \tag{IV.4}$$

Where: N is the number of carbon pairs in the unit cell.

Also, the wave vector in the Brillouin zone of a semiconductor-type nanotube can be obtained from the following relation:

$$K = \frac{2\pi\sqrt{3}j - n_1ka}{2an_1}\hat{X} + \frac{2\pi j + \sqrt{3}n_1ka}{2an_1}\hat{Y} \tag{IV.5}$$

By substituting (5) into the graphene dispersion relation, we can obtain the dispersion relation for a semiconductor nanotube as follows:

$$E(k) = \pm t\sqrt{1 + 4cos\left(\frac{\sqrt{3}ka}{2}\right)cos\left(\frac{j\pi}{n_1}\right) + 4cos^2\left(\frac{j\pi}{n_1}\right)} \tag{IV.6}$$

Where: J is the number of subbands, given by:

$$j = round\left(\frac{2n_1}{3}\right), round\left(\frac{2n_1}{3}\right) + 1, \ldots\ldots, (2n_1 - 1) \qquad \textbf{(IV}.7)$$

Thus, the minima of the 1st, 2nd, ..., jth subband represent the lowest energy of each subband. Therefore, the number of effective subbands can be determined by comparing the positions of the subband minima with the Fermi level.

b. Calculation of the charge density

The induced charge density (electrons or holes) plays a crucial role in defining the behavior of carbon nanotube-based devices. The charge generated by the gate voltage V_{gs} within the CNTFET channel moves between the source and drain, producing the drain current I_d. The charge density for each subband can be calculated using the following relation [10]:

$$N_e(E) = \int_{-\infty}^{\infty} D_{NT}(E)F(E - E_F)dE \qquad \textbf{(IV}.8)$$

Where: $F(E - E_F)$ is the equilibrium Fermi function and $D_{NT}(E)$ is the density of states at the top of the barrier of the 〖p〗^thnanotube subband, the latter is given by:

$$D_{NT}(E) = g_0 \frac{E - E_0}{\sqrt{(E - E_0)^2 - \Delta_P^2}} \qquad \textbf{(IV}.9)$$

Where:Δ_P is theP^{th} subband minimum, E_0 is the mid-gap energy, and g_0 is the metallic density of states. When a voltage is applied to the gate and drain terminals, the states are occupied according to two different Fermi levels. Consequently, the total number of electrons (N_t) in the channel as a function of energy can be written as follows:

$$N_t(E) = \int_{E_c}^{\infty} D_{NT}(E - U_{SCF}) \frac{f_1(E) + f_2(E)}{2} dE \qquad \textbf{(IV}.10)$$

Where $f_1(E)\ and\ f_2(E)$ are the Fermi function for the Fermi levels E_{F1} and E_{F2}, respectively, and U_{SCF} is the channel potential at the top of the barrier, given by the following equation:

$$U_{SCF} = \left[U_L + \frac{q^2 N}{C_\Sigma}\right] \qquad \textbf{(IV}.11)$$

In order to calculate the total number of electrons, it is necessary to know the channel potential (U_{SCF}), At the same time, the total number of electrons is essential to calculate the channel potential, therefore, we use the self-consistent method to obtain the total number of electrons. Thus, we can calculate the total induced number in the channel at the sub band(ΔN) by substituting (**IV**.7) and (**IV**.9) into (**IV**.8).

$$\Delta N = g_0 \int_0^{\infty} \left[\frac{dZ}{1+exp\left[\frac{\sqrt{Z^2+\Delta_P^2}+(\Delta_n-\Delta_p)}{K_B T}\right]} + \frac{dZ}{1+exp\left[\frac{\sqrt{\Delta+\Delta_P^2}+(\Delta_n-\Delta_p)}{K_B T}\right]} \right] \quad \textbf{(IV.11)}$$

With : $$Z = \sqrt{(E - E_{CP} + \Delta_P)^2 + \Delta_P^2} \quad \textbf{(IV.12)}$$

The calculation of the current-voltage (I-V) characteristics of the OG-CNTFET in the ballistic regime is related to the number of contributing subbands. The net current per subband in the nanotube is given by [8]:

$$I_d = \frac{4e}{\hbar} \int_{-\infty}^{+\infty} \frac{dE}{2\pi} T(E)[f_1(E) - f_2(E)] \quad \textbf{(IV.13)}$$

With the transmission coefficient T(E) given by:

$$T(E) = Trace[G_1(E)G(E)G_2G^+(E)] \quad \textbf{(IV.14)}$$

Modeling CNTFETs requires a solid foundation in quantum mechanics. The non-equilibrium Green's function method, along with the Landauer formalism, has been applied to compute the charge current (both electrons and holes) within the nanotube. The current-voltage characteristic curve can be divided into two operating regions: linear and saturation. Mr. D. S. Hien provided the expression for the drain current in the linear regime directly as follows:

$$I_d = \frac{W}{L} \mu C_{ox} \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad \textbf{(IV.15)}$$

$$I_d = K_n \left[2(V_{gs} - V_T) V_{ds} - V_{ds}^2 \right] \quad \textbf{(IV.16)}$$

C_{ox} represents the capacitance of the oxide layer located above the gate, and in the case of a planar CNTFET, it is expressed by the following relation:

$$C_{OX} = \frac{2\pi\varepsilon}{log(2t_{ox}/d)} \quad \textbf{(IV.17)}$$

Where: S is the surface area of the oxide layer and d its thickness, k: the relative permittivity of the oxide, and ε: the permittivity of free space.

Kn is the conductance of the CNTFET, W is the width of the CNTFET, L is the length of the CNTFET, μ is the carrier mobility, and C_{ox} is the gate oxide capacitance.

We can also obtain the current in the saturation regime quite simply by replacing V_{ds} (sat) with V_{gs} - V_T. Then, the expression for the saturation current of the CNTFET can be written directly as follows [8]:

$$I_{d(sat)} = K_n\left(V_{gs} - V_T\right)^2 \qquad \text{(IV.18)}$$

IV.2.2. Channel modulation by illumination

To calculate the change in drain current under the influence of light, we based our work on the research of Si-Yu LIAO and the research team from the University of Bordeaux 1, France. [11], who developed an analytical and simulation study of the optoelectronic characteristics of OG-CNTFET transistors, then we incorporated the results of this study into the basic I-V characteristic model presented earlier.

IV.2.2.1 Analysis of optical modulation

At room temperature, the conductance of a single-walled carbon nanotube (SWNT) is highly sensitive to its electrostatic environment. Taking advantage of this electrical charge sensitivity, non-volatile memories based on CNTFETs have been developed by trapping charges in the gate oxide. The operating principle of the OG-CNTFET is similar. When an OG-CNTFET is illuminated with an appropriate wavelength, electron-hole pairs are generated within the polymer. A small fraction, less than 5%, of these photo-generated electrons gets trapped in the P_3OT material. If the transistor is electrically blocked by the gate (with a positive V_{GS}), the photo-generated electrons are attracted by the electric field from the gate and become trapped at the P_3OT-SiO_2 interface over the illuminated area. These trapped electrons near the nanotube contribute to modulating the channel potential (**Figure IV**.2). In fact, the charge represented by these electrons is located very close to the gate. As a result, the modulation effect of the gate is screened by that of the electrons (**Figure IV**.1). This phenomenon is referred to as "Optical Gating".

When the illumination is turned off, the trapped electrons do not recombine immediately. The "Optical Gating" effect lasts for more than a day. This behavior can be regarded as non-volatile memory for electronic applications operating at frequencies on the order of kilohertz. The phenomenon is governed by the electrochemical trapping mechanism of electrons by the OH complex in the form of the reduction of SiOH, which charges the P_3OT-SiO_2 interface as a layer of fixed negative ions.

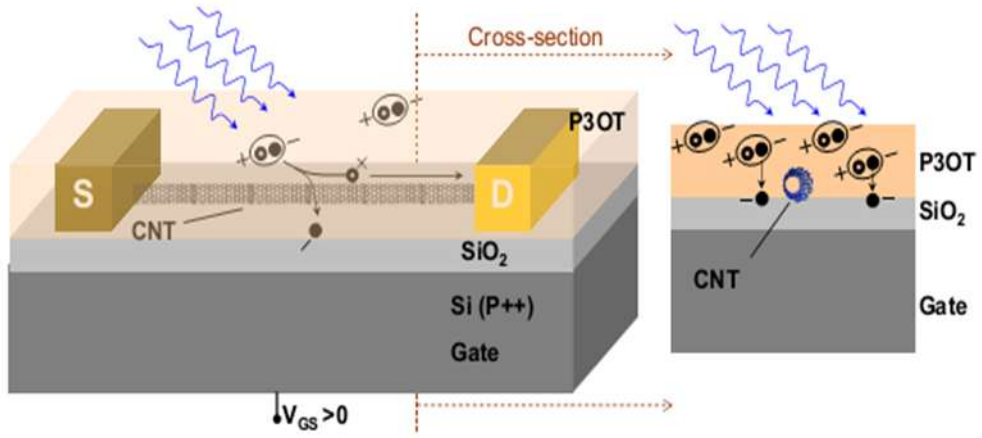


Figure IV.2. *Représentation schématique de la dynamique de l'effet "Optical Gating" dans un OG-CNTFET [12].*

IV.2.2.2 Modeling of optical modulation

The modeling of the optical control of the OG-CNTFET is introduced by considering the influence of trapping at the P_3OT-SiO_2 interface on the modulation of the transistor's channel potential. The method begins by determining the amount of trapped electrons.

Modeling of the optical absorption of P_3OT

To determine the quantity of trapped electrons, it is first necessary to find the amount of photo-generated electrons in the polymer. The absorption of P_3OT characterizes the efficiency of converting photons into photo-generated electron-hole pairs. It exhibits wavelength selectivity for the incident light. According to the literature, the wavelengths used to excite the samples range from 450 to 700 nm, corresponding to the red to blue range in the visible spectrum [5]. The absorption of P_3OT exhibits a Gaussian shape within this wavelength range [5,7,13]. In line with these experiments, we modeled the absorption of P_3OT using the following equation as a function of λ_{lazer} :

$$\alpha_{P3OT} = \alpha_0 \exp\left(-\gamma(\lambda_{lazer}-\lambda_0)^2\right) \qquad (\textbf{IV}.19)$$

- α_0 : is the maximum of the Gaussian, equal to 0,0366.
- λ_0 **:** is the central wavelength, equal to 442,8 nm**.**
- The coefficient fixes the width equal to $1{,}45\times10^{14}$ nm^{-2}.

This experimental model is compared with the numerical model [5] shown in **the figure IV.3.**

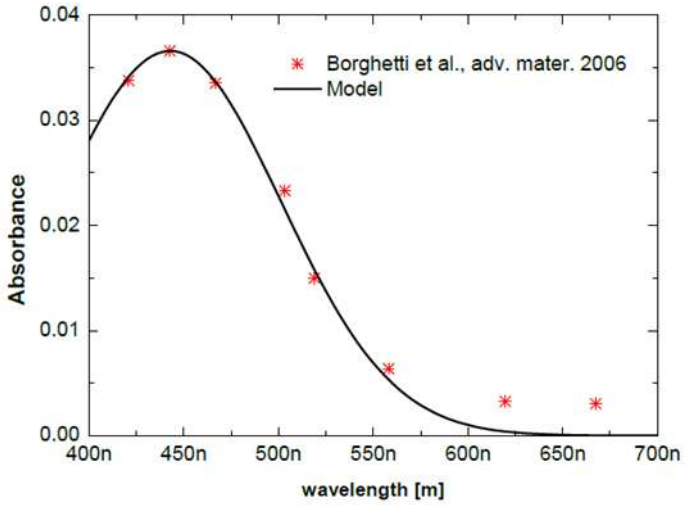


Figure IV.3. *Validation of the experimental model of the optical absorption of P_3OT [10].*

Modeling of electron traps at the P_3OT/SiO_2 interface

The trapping of photo-generated electrons in the P_3OT at the SiO_2 interface can be interpreted as trap charges at the P_3OT-SiO2 interface. As a first approximation, these traps can be modeled as a series of capacitors between the P_3OT-SiO_2 interface and the back gate, as shown in Figure **IV**.2. The oxide layer thickness is estimated to be around 1 nm. The photo-generated trapped electrons are assumed to be uniformly distributed over the illuminated region. However, only those located near the nanotube channel are capable of modulating the transistor's conductance that is, within an effective zone surrounding the nanotube at the interface. The electric field distribution caused by the trapped charges in this effective area can be approximated by a uniform field generated by a charged region near the nanotube with a width of about 10 nm. It should be noted that electrons trapped very close to the channel immediately dissipate through the nanotube.

Based on this approximation, the capacitive network can be simplified into two capacitors in series. One is between the CNT and the charge zone, and the other is between the charge zone and the gate. These elements are in parallel with the gate oxide capacitor C_{OX}. Moreover, these additional elements should not alter the operation when the transistor is not illuminated. In other words, the series capacitors must be much smaller compared to C_{OX}. This is a realistic consequence because the capacitance between the traps and the gate must be very low to represent a good gate oxide [14].

Modeling of the current source dependent on optical power

To link the quantity of photo-generated electrons in the P_3OT and the equivalent capacitors representing the interface traps, a current source is necessary. This current source is modeled by describing the light power as photo-generated electrons that charge the equivalent capacitors. The current is expressed as:

$$I_{Optic} = \frac{dn_{trapped}}{dt} = \frac{dn_{photon-genertedd}}{dt} . rate_{separation} . \frac{A_{eff}}{A_{SPOT}} \qquad \textbf{(IV}.20)$$

Where $n_{trapped}$ and$n_{photon-genertedd}$ are the densities of trapped photo-generated electrons and photo-generated electron-hole pairs in the P_3OT, respectively $rate_{separation}$ is the separation rate of the photo-generated electron-hole pairs.A_{eff} and A_{SPOT} are the areas of the effective trap zone and the size of the light spot, respectively. This ratio gives the percentage of the number of pairs in the effective zone.

The total quantity$n_{photon-genertedd}$ differentiated with respect to time is expressed as:

$$\frac{dn_{trapped}}{dt} = \frac{eP_{Laser}}{h\nu_{Laser}} = \frac{eP_{Laser}\lambda_{Laser}}{hc} \qquad \textbf{(IV}.21)$$

Where P_{Laser},$\nu_{Laser}$and $\lambda_{Laser}$are the light power, frequency, and wavelength of the incident laser. The ratio of the power $P_{Laser}$to the energy of a photon $h\nu_{Laser}$gives the number of photons incident per unit time. Thus, the current dependent on the optical power and parameterized by the wavelength of the incident light becomes:

$$I_{Optic} = \frac{eP_{Laser}\lambda_{Laser}}{hc} . \alpha_{P3OT}(\lambda_{Laser}) . rate_{separation} . \frac{4\mathcal{W}_{eff}L_G}{\pi\, d_{spot}^2} \qquad \textbf{(IV}.22)$$

Where:

$\mathcal{W}_{eff}$: is the width of the effective zone.

d_{spot} : is the diameter of the light spot.

Modeling of the 'optical control' incorporating non-volatile memory effect

Before modeling the optical control, it is important to assess how the P_3OT independently affects the electrostatic environment of both the nanotube and the transistor. Depositing P_3OT effectively acts as a p-type doping for the intrinsic nanotube and leads to changes in the electrostatic capacitances on the drain and source sides. This impact is clearly demonstrated by comparing the I_{ds}-V_{gs} characteristics of a transistor before and after the P_3OT deposition. However, this study utilizes s-SWNTs with a purity exceeding 97% [15], This doping effect is not significant in the samples presented by CEA-LEM. We can conclude that, by combining negative charges caused by impurities trapped at the P_3OT-SiO_2 interface near the nanotubes

[16], P_3OT electrostatically dopes these s-SWNTs. In our compact model, a parameter called doping P_3OT quantifies this doping in cm^{-1}.

The optical current source and the equivalent capacitors representing interface traps are modeled. These elements are incorporated into the compact model of a conventional CNTFET to replicate the effect of optical control. The equivalent circuit diagram for trap charging is shown in Figure **IV**.4.

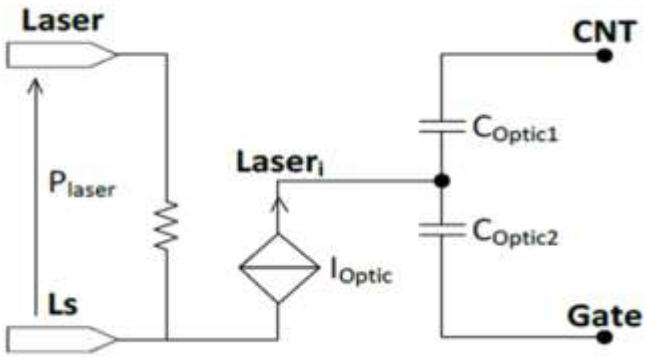


Figure IV.4. *Simplification of the capacitor network in the active area for optical modeling [10].*

The nodes Laser and Ls are two virtual nodes that represent the input optical power of the circuit. The values at the Laser and Ls nodes are fixed to Plaser and zero, respectively. The CNT and Gate nodes correspond to the nanotube channel and the gate, respectively. I_{Optic} is the modeled current source. C_{Opticl}represents the equivalent capacitor between the nanotube and the interface electron traps. In this study, the value of $C_{Opticl}$is about ten times greater than that of C_{OX} . $C_{Opticl2}$is the equivalent capacitor between the interface traps and the gate. Its value is negligible (between 1% and 5%) compared to C_{OX} to reflect the realistic assumption regarding the relative significance of C_{OX} in relation to the interface trap capacitance. Therefore, the combined value of $C_{Opticl1}$ and $C_{Opticl2}$ (in series) is negligible compared to C_{OX} .

When the transistor is not activated, this part does not affect the channel potential. However, when the OG-CNTFET is illuminated, the current sourceI_{Optic} converts the incident light power, based on its wavelength, into separated photogenerated electrons. These electrons gradually charge the trap capacitors $C_{Opticl1}$ and $C_{Opticl2}$. The accumulated charges cause changes in the potentials of the nanotube channel (CNT node) and the gate (Gate node), respectively. Once the illumination ceases, the charging process also stops.

A note on the modeling is the nonlinearity of the optical control effect. The modulation as a function of optical power is neither linear nor exponential. This relationship remains undetermined. We assume a linear conversion of the optical power into charges within the channel (eq. **IV**.22).

The amount of charge stored in the capacitors remains constant. Thus, we have represented the effect as a theoretically infinitely long non-volatile memory.

The study of charge balance in operation explains the mechanism behind the modulation of the channel potential induced by optical control. In a conventional CNTFET, the channel potential is modulated by the field effect generated by the gate, as well as by charges originating from the drain and the source [17,18]. For an OG-CNTFET, the potentialV_{CNT} is expressed according to the following charge balance (**Figure IV**.4):

$$\Delta Q = C_{OX}(V_G - V_{CNT}) + C_{DE}(V_D - V_{CNT}) + C_{SE}(V_S - V_{CNT}) + C_{Opt}(V_{Laser} - V_{CNT}) \ldots$$
(**IV**.23)

With V_G, V_D, V_S and V_{Laser} The potentials at the gate, drain, source, and Laser nodes, respectively. $C_{DE}$and C_{SE} are the electrostatic capacitances on the drain and source sides. ΔQ is the charge density in the channel at zero bias. In equation (**IV**.23), the four product terms represent the charges from the gate, drain, source, and optical control, respectively. Finally, the value V_{CNT} of is derived as:

$$V_{CNT} = \frac{(C_{OX} V_G)+(C_{DE}V_D)+(C_{SE}V_S)+(C_{Opticl}V_{Laser})-\Delta Q}{C_{OX}+C_{DE}+C_{SE}+C_{Opt}} \qquad (\mathbf{IV}.24)$$

One point to note in the modeling is the nonlinearity of the optical control effect. The modulation as a function of optical power is neither linear nor exponential [5]. This relationship remains undetermined. We assume a linear conversion of optical power into charges within the channel (eq. **IV**.24).

IV.3. Total drain current

The total drain current I_{tot} is the sum of the two previously calculated currents: the dark current I_d, resulting from the applied bias voltages the drain voltage V_{DS} and the gate voltage V_{GS} [equations **IV**.15 and **IV**.18] and the optical current I_{op} [equation **IV**.22]. The expression for the total current is given by the following relation:

$$I_{tot} = I_d(\text{in darkness}) + I_{op} \qquad (\mathbf{IV}.25)$$

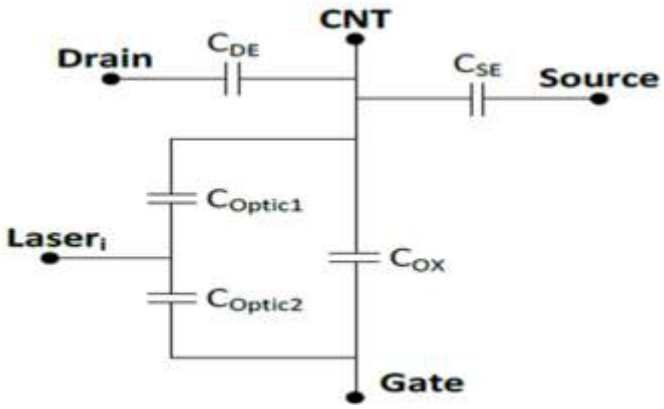


Figure IV.5. *Schematic overview of the charges that modulate the channel potential in the OG-CNTFET [10].*

IV.4. Simulation program

To validate the mathematical model established in the second chapter, a simulation program was developed using Fortran Power Station 90 version 4.0. This program, based on the various formulas and equations presented in the second chapter, allows translating all these equations into numerical tables. Using these tables and with the help of Origin software version 6.1, we can plot and present the different series of results and curves.

a) b)

Figure IV.6. *Software used: a) Fortran Power Station version 4.0, b) Origine version 6.1*

The established algorithm to calculate the electronic and optoelectronic characteristics of the studied components is shown in Figure **IV**.2.

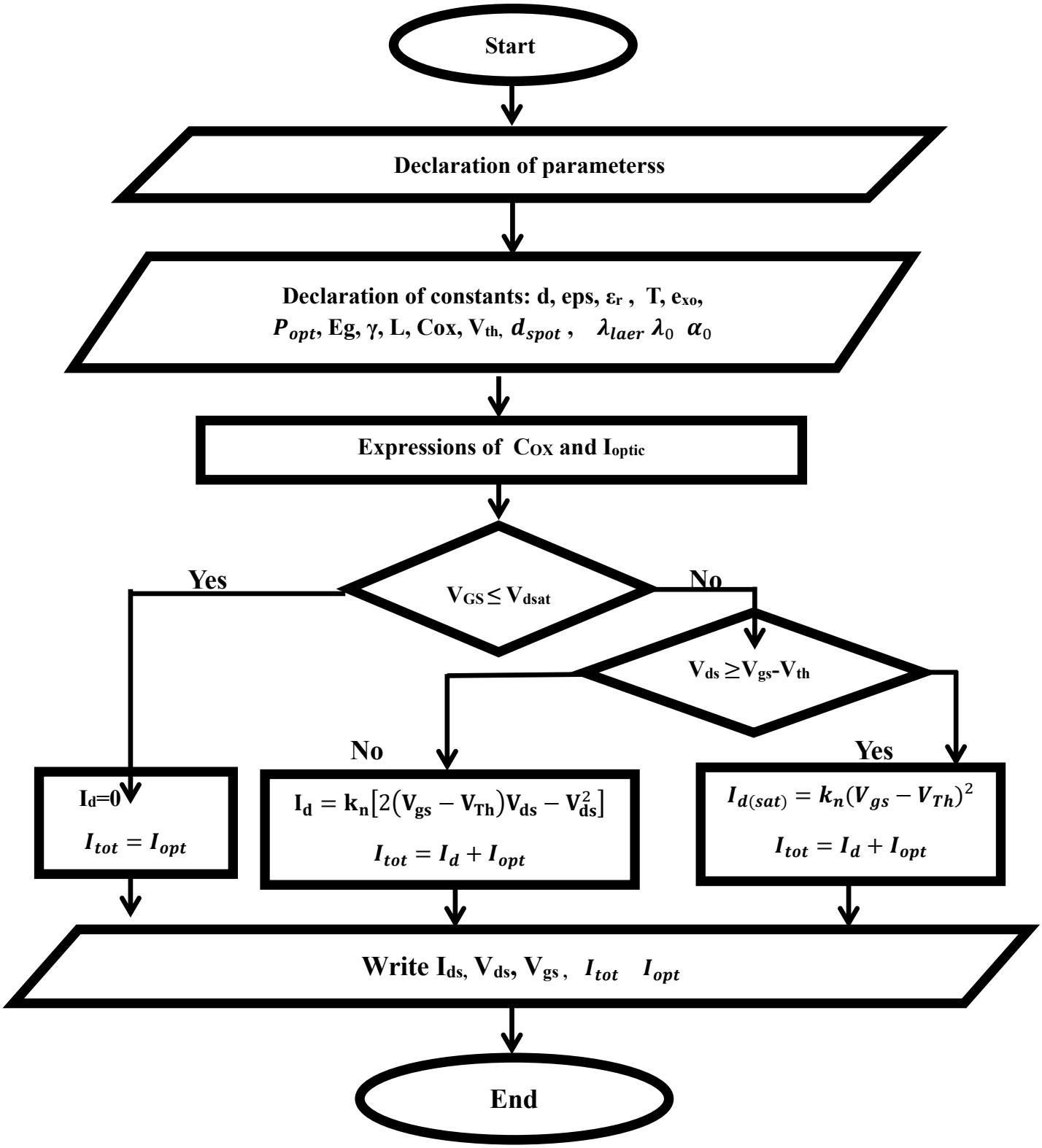


Figure IV.7. *Calculation flowchart.*

IV.4.1. Caractéristiques courant tension I-V

To present the results of our work, and based on the expressions established in the second chapter, specifically expressions (**IV** -3), (**IV** -12), (**IV** -13), (**IV** -14), (**IV** -15), and (**IV** -16), we perform the numerical simulation of the drain current I_{ds}as a function of the gate bias voltages V_{GS} and drain V_{DS} in the different operating regimes of the transistor.

The geometric and technological parameters of the OG-CNTFET transistor, along with the parameters of the light spot (laser) that we used, are grouped in the following tables:

Table IV.1. Parameters used in the study.

Diameter of the CNT	Gate length	Threshold voltage	Relative permittivity of the oxide	Oxide thickness
d	L	V_{th}	ε_r	e_{ox}
1.5 nm	100 nm	0.2 V	3.9	5 nm

Diameter of the light spot	Central wavelength	Laser wavelength
d_{spot}	λ_0	λ_{laer}
1 µm	0.4428 µm	450 nm

Gaussian	Width of the effective area	Optical power	Temperature
α_0	W_{eff}	P_{opt}	T
0.0366	100 nm	50 mW	300° K

In the following paragraphs and figures, we will present the set of I-V characteristics of the OG-CNTFET nanotube transistor. These characteristics describe the variation of the drain current « I_{ds}» as a function of the drain voltage «V_{ds}» for different values of the gate voltage «V_{gs} ».

In **Figure** (**IV**.**8**) we have presented the characteristic I_{ds} as a function of V_{ds} for different parameters of V_{gs}. We can characterize the three zones that represent the different operating regimes of the transistor.

- ✓ The linear zone (ohmic region): the drain current I_{ds} varies almost linearly as a function of the drain voltage V_{ds}; it corresponds to the linear operating regime.

- ✓ The pinch-off region: the drain current I_{ds} increases but not in a linear way until it reaches its saturation value.
- ✓ The third zone, called the saturation operating region, corresponds to the condition: $V_{ds} > V_{dsat}$ Where the drain current is independent of the drain voltage.

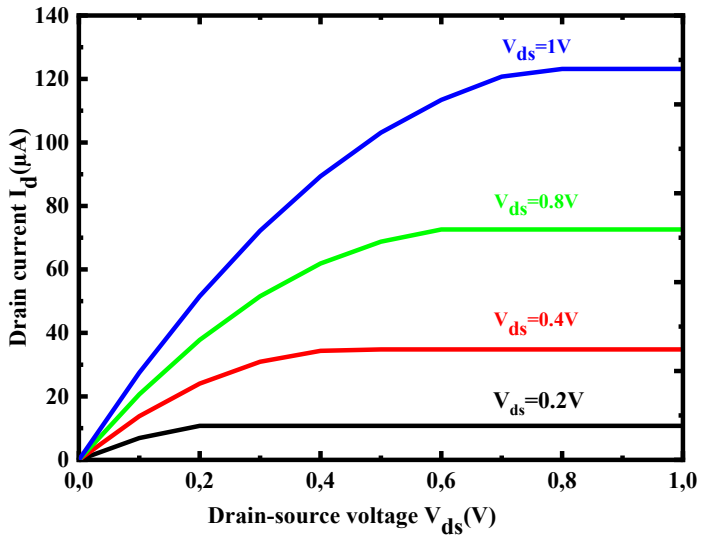


Figure IV.8. *Network of current-voltage characteristics I_{ds}-V_{ds} of the studied component*

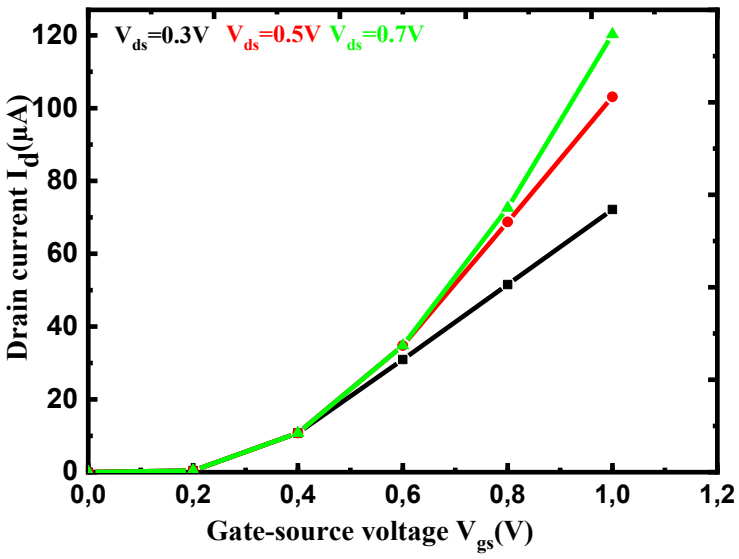


Figure IV.9. *Variation of the drain current as a function of the gate voltage for several values of the drain voltage.*

Description of the three zones*:*

- **The linear region :**

When the voltage V_{gs} exceeds the threshold voltageV_{th} A larger quantity of electrons is attracted into the channel. One can visualize the influence of the voltage V_{gs} (above V_{th}) (such as an increase in the channel depth. This results in an increase in the channel conductance, that is, a reduction in its resistance. The current Id flowing through the channel is therefore proportional to ($V_{gs} - V_{th}$) and to the applied Drain-Source voltage, see **Figure IV**.3. And increases proportionally to V_{ds}, and the shape of the characteristic is quasi-linear.

- **The pinch-off region:**

We observe that the Drain-Source voltage V_{ds} actually appears as a voltage drop along the entire channel. As a result, the voltage between the gate and various points along the channel is variable, from V_{gs} on the Source side to $V_{gs} - V_{ds}$ on the Drain side. Since the channel depth depends on this voltage, it is clear that the channel depth is not uniform. As the Drain-Source voltage V_{ds} increases, the channel develops an increasingly steep gradient and its resistance increases. When the Drain-Source voltage V_{ds} reaches a value such that the the gate-to-channel voltage on the Drain side reaches the threshold voltage, that is: V_{gs} - V_{ds}= V_{th} hence V_{ds}= V_{gs}-V_{th}. The channel depth at the Drain end approaches zero; this is referred to as pinch-off.

- **The saturation region:**

In this region, any increase in the drain voltage V_{ds} beyond the pinch-off region will have no effect on the drain current intensity I_{ds}, in this context, the current may be designated as I_{ds} by I_{dsat}, or simply, the saturation current.

IV.6.2. Effect of various parameters on the photocurrent (optical current)

Optical excitation has a significant impact on certain carbon nanotube-based components, particularly the OG-CNTEFT transistor. The electrical current resulting from this influence is referred to as the photocurrent or optical current (expression **IV** -22). In the following sections, we present the effect of this current on the device characteristics. I_{ds}-V_{ds} of the studied OG-CNTFET device, as well as the effect of several parameters on the optical current itself.

IV.4.2.a. Effect of optical power on the photocurrent

To examine the effect of optical power (emitted by a laser diode) on the photocurrent of the CNTFET transistor, we studied the variation of the photocurrent as a function of several

values of the optical power (ranging from 10 mW to 100 mW). The simulation results are presented in **Figure IV.10**. This figure illustrates that the relationship between the two quantities is linear, where the photocurrent within this range increases linearly with the optical power produced by the laser.

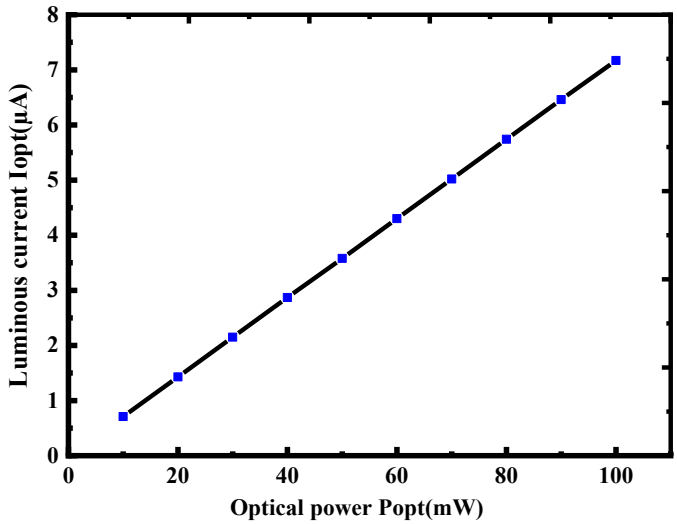


Figure IV.10. *Relationship between optical power and photocurrent generated in the OG-CNTEFT.*

IV.4.2.b. Effect of wavelength on the photocurrent

Figure IV.11 depicts the influence of the wavelength of the laser used λ_{laser} on the variation of the optical current I_{opt}. In this figure, we can identify three distinct operating regions in which the optical current exhibits specific behavior : The perimeter zone (λ_{laser} = 0.4 µm to 0.44 µm) : It is observed that current I_{opt} increases when λ_{laser} augmente. The second zone (λ_{laser} = 0.44 µm): the currentI_{opt} reaches its maximum value at 5.3 µA . The third zone (λ_{laser} = 0.44 µm to 0.5 µm): We observe the current I_{opt} decreases despite the wavelength « λ_{laser} » increases. From this figure, we observe that the photocurrent in the studied OG-CNTFET component can only exist within a narrow band of characterized light.

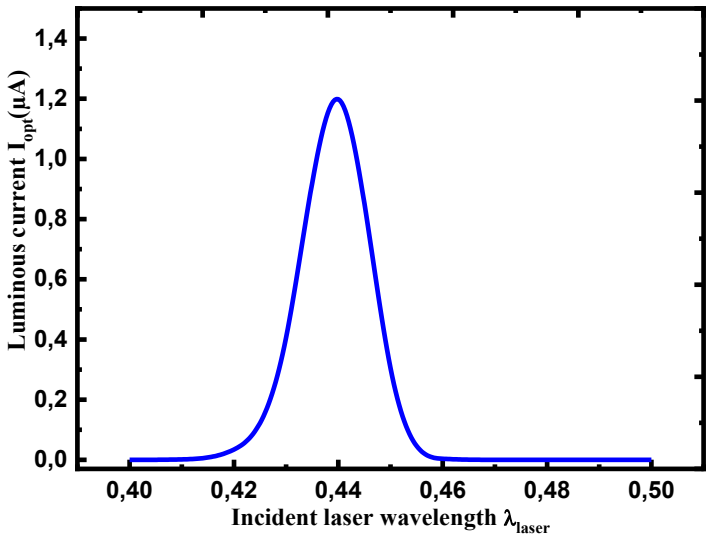


Figure **III.11.** Effect of the laser wavelength on the photocurrent in the studied OG-CNTFET.

IV.4.2.c. Effect of the surface on the photocurrent

The effective surface is the one under the gate that is exposed to the light $S_{eff} = W_{eff} . L$, where W_{eff} "is the effective width of the top surface of the component and L is the length of the gate. To examine the effect of this surface on the photocurrent, we have presented in **Figure IV.12** the variation of the drain current as a function of the width W_{eff} (W_{eff} varies from 50 to 200 nm) effective because the gate length is fixed ($L = 100\ nm$). The figure shows that the relationship between the surface exposed to light and the generated photocurrent is similar: if the surface increases, the current also increases, and vice versa.

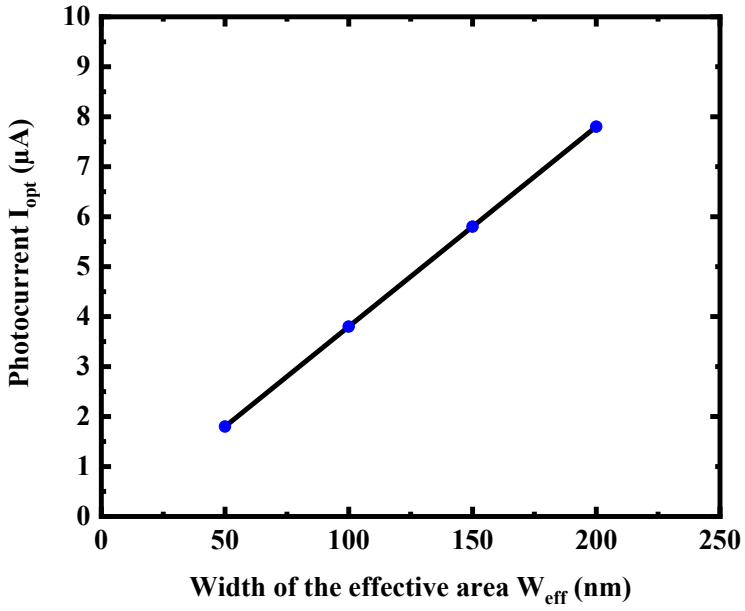


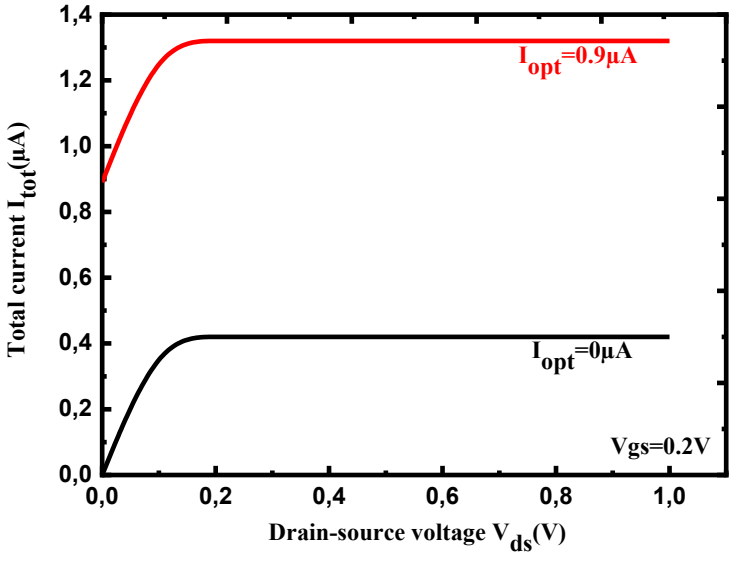
Figure IV.12. *Effect of the width of the effective area on the photocurrent of the OG-CNTFET.*

IV.5. Total current

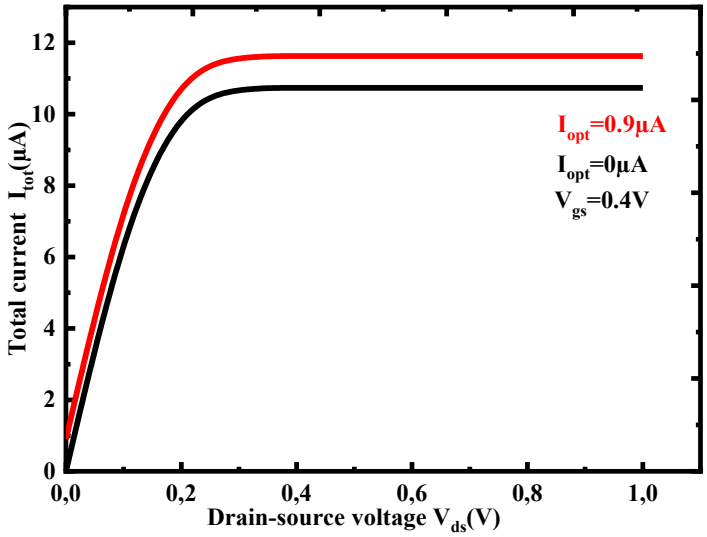
The total current « I_{tot}» It is the drain current under the influence of light, so it represents the sum of the drain current in darkness and the optical current resulting from optical excitation (expression **IV**.26). In the following paragraphs, we will present this optical current and examine the influence of some parameters such as the gate voltage.

V_{gs}, the optical excitation power and the laser wavelength on the characteristic I_{tot}-V_{ds}.

Figure IV.13 represents a comparison of the characteristic I_{ds}-V_{ds} in darkness and under optical excitation (total current) for two values of the gate voltage: (a) V_{gs} = 0,4 V and (b) V_{gs} = 0,8 V , These two figures show that the difference between the two currents exists at all points of the drain voltage V_{ds} in both cases is significant, because the optical current in this case is equal to *3,5 µA*, This value is higher than that of the saturation current in darkness for V_{gs} = *0,4* V and represents a remarkable difference for V_{gs} = 0.8 V. This result shows that the optical current has an influence that cannot be neglected and must be taken into consideration in all applications of OG-CNTFET transistors in various fields of technology.



(a)



(b)

Figure IV.13 *Comparison between the total drain current (above) and the drain current in darkness (below): (a) for V_{gs} = 0.4 V and (b) for V_{gs} = 0.8 V.*

IV .5. 1. Effect of optical power on the total current

To examine the effect of optical power on the total current of the studied OG-CNTFET transistor, we presented in Figure (**IV**.14) the total current versus drain voltage characteristic I_{tot}-V_{ds} for V_{gs} = *0,6* V for three different values of optical power (P_{opt} = 10, 50, and 100 mW). This figure reaffirms the correlation between the optical excitation power and the optical current

produced in the component, and consequently, the correlation between the power and the total drain current.

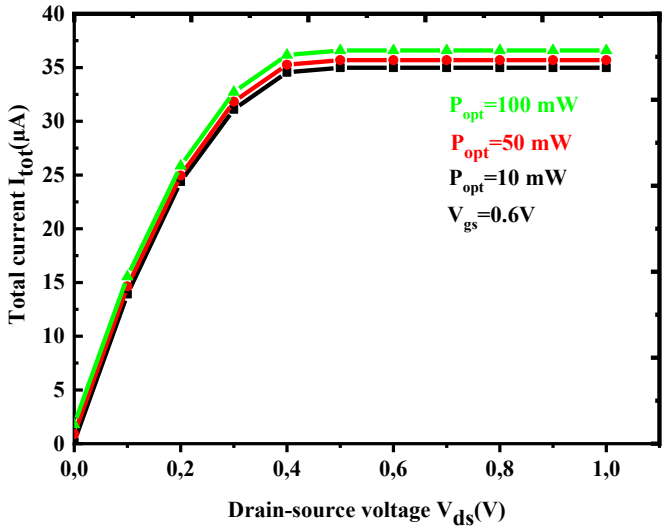


***Figure IV** -14: Characteristic I_{tot} =f (V_{ds}) for different values of optical powers.*

IV .5. 2. Effect of wavelength on the total current

Figure (**IV**.15) shows the I_{tot}-V_{ds} characteristic at a gate voltage of V_{gs} =*0.4 V* for three different values of the wavelength (λ = *43, 44, 45*μm). This figure also reaffirms that the optical current is more sensitive to certain wavelengths than others. In the case studied in this figure, we observe that the current corresponding to λ = *44* μm is higher than the currents corresponding to λ = *43* μm and λ = *45* μm. This characteristic confirms that each optoelectronic component is sensitive to a typical wavelength, which is very important, especially in the field of telecommunications

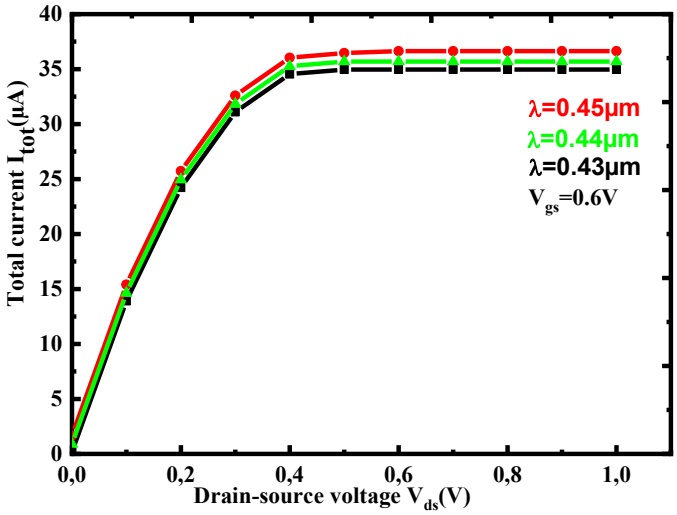


***Figure IV** -15: Characteristic I_{tot} =f (V_{ds}) for different values of the wavelength.*

IV.6 Conclusion

In this chapter, we present a simulation study of the static characteristics and optoelectronic characteristics of an OG-CNTFET transistor. The chapter consists of three parts: the first part is dedicated to the current-voltage characteristics of the OG-CNTFET component, where we observed that the OG-CNTFET exhibits characteristics similar to other field-effect transistors such as the MOSFET and other CNTFETs. The second part of the chapter is reserved for the study of the optoelectronic characteristics of the OG-CNTFET component, a characteristic that is proprietary to this component and opens great possibilities for using this type of device, especially in the field of optoelectronics and telecommunications in the next generations of broad range electronic devices. The third part presents the influence of light excitation on the static characteristics of the OG-CNTFET component, where we consider this influence to be very significant and not negligible. Finally, we note that this study is important for the design and use of OG-CNTFET type components in various technological fields.

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V. Introduction

Two-dimensional (2D) materials have revolutionized nanoelectronics and sensing technologies due to their unique physical, chemical, and electronic characteristics that do not appear in bulk materials [1]. These ultrathin materials exhibit atomic-scale thickness and high surface to volume ratios, which lead to exceptional electrical and mechanical properties [2]. Among them, graphene, a monolayer of carbon atoms arranged in a hexagonal honeycomb lattice is the prototypical 2D material, notable for its extremely high carrier mobility, excellent mechanical strength, and remarkable thermal conductivity [3]. Nevertheless, the absence of an intrinsic electronic bandgap in pristine graphene restricts its applicability in electronics that require high switching ratios and in sensing platforms demanding enhanced signal to noise performance [4].

Graphene nanoribbons (GNRs) are narrow strips derived from graphene that retain many of graphene's excellent properties while exhibiting width- and edge-dependent tunable bandgaps due to lateral quantum confinement and edge effects [5,6]. This bandgap tunability effectively transforms GNRs from semi-metallic to semiconducting materials, enabling their use in transistor channels with desirable on/off switching capabilities [5]. The edge morphology, specifically armchair or zigzag configurations, is a critical factor influencing GNR electronic, magnetic, and transport properties; armchair edges predominantly impact the bandgap size, whereas zigzag edges introduce localized edge states with potential magnetic behavior [6,7]. These features provide a versatile platform for band structure engineering critical to nanoelectronic and sensing device design [8]. The enhanced surface-to-volume ratio and presence of chemically accessible edges in GNRs dramatically increase their interaction with the environment, positioning them as outstanding candidates for gas and chemical sensors [9]. Gas sensors based on graphene nanoribbon field-effect transistors (GNRFETs) exploit adsorbate-induced charge transfer processes that modulate the electrical conductivity of the transistor channel, offering highly sensitive and rapid response detection capabilities suited for environmental monitoring and industrial applications [9,10].

However, traditional single-gate GNRFETs face limitations such as suboptimal electrostatic gate control and pronounced short-channel effects when device dimensions shrink, which hamper device performance and scalability. To address these challenges, double-gated GNRFET architecture featuring independent top and back gate electrodes separated by dielectric layers have been developed to provide enhanced electrostatic control and improved

switching behavior. This configuration leads to stronger capacitive coupling, suppression of leakage currents, and superior tunability of carrier density within the GNR channel, thereby improving sensitivity, I_{on}/I_{off} ratio, and overall device reliability.

A critical enabler of this improved gate control is the use of high-k dielectric materials, particularly lanthanum aluminate ($LaAlO_3$), as the gate dielectric layer. $LaAlO_3$ exhibits a high dielectric constant (~30), excellent thermal stability [11], and chemical inertness that surpass traditional dielectrics like SiO_2 or Al_2O_3. These properties facilitate stronger capacitive coupling between gate and channel, enabling substantial modulation of carrier density at reduced gate voltages while minimizing leakage currents and power consumption an essential features for low-power sensor devices. The robust nature of $LaAlO_3$ also enhances device stability and longevity under varying environmental and operational conditions [12,13].

The unique aspect of our work is the integration of $LaAlO_3$ dielectric layers on both top and back gates, forming a double-gated GNRFET sensor with the GNR channel sandwiched between these high-k dielectric layers. This design affords unprecedented electrostatic control, enabling highly sensitive and selective detection of ammonia (NH_3) gas molecules a pollutant of significant environmental and health concern. We systematically explore how key parameters, such as NH_3 gas concentration, back gate voltage, temperature, and the thicknesses of both $LaAlO_3$ top and back gate dielectrics, influence critical performance metrics including drain current (I_d) and I_{on}/I_{off} ratio. Our results reveal how tuning these parameters can optimize the sensor's electrical response, sensitivity, and stability, surpassing the performance of existing single-gate or low-k dielectric-based devices.

Additionally, the double-gated architecture offers flexibility for post-fabrication device tuning, allowing adjustment of detection limits and sensitivity ranges tailored to specific application needs. This adaptability, combined with the high quality dielectric interface provided by $LaAlO_3$, positions our sensor as a promising candidate for scalable, compact, and energy efficient gas sensing platforms in environmental monitoring and IoT integration.

This chapter advances the field of 2D material-based gas sensors by leveraging the synergistic advantages of graphene nanoribbons as tunable semiconducting channels, double-gated transistor architecture for enhanced electrostatic control, and high k $LaAlO_3$ dielectrics for efficient gating. The findings provide valuable insights into optimizing electrical and sensing performance, paving the way for practical implementation of high performance, low-power, and scalable GNRFET gas sensors.

V.1 FET-Based Structure

As illustrated in **Figure V.1**, the proposed graphene nanoribbon field-effect transistor (GNRFET) exhibits a structural configuration closely resembling a conventional double-gate metal-oxide-semiconductor field-effect transistor (MOSFET). The device comprises source and drain contacts bridged by a graphene channel, with a top gate electrode designed to modulate carrier transport within this channel. A dielectric layer electrically isolates the top gate from the channel, and to enhance electrostatic gate control and mitigate short-channel effects, the gate partially overlaps the channel region. It is important to note that, within the context of gas sensing, the gate primarily serves to regulate the channel conductivity rather than to directly interact with or absorb gas molecules [14]. To improve sensitivity by facilitating gas molecule adsorption near the channel surface, high-k dielectric materials such as lanthanum aluminate ($LaAlO_3$) are employed for the gate dielectric, despite the partial coverage of the channel by the gate structure.

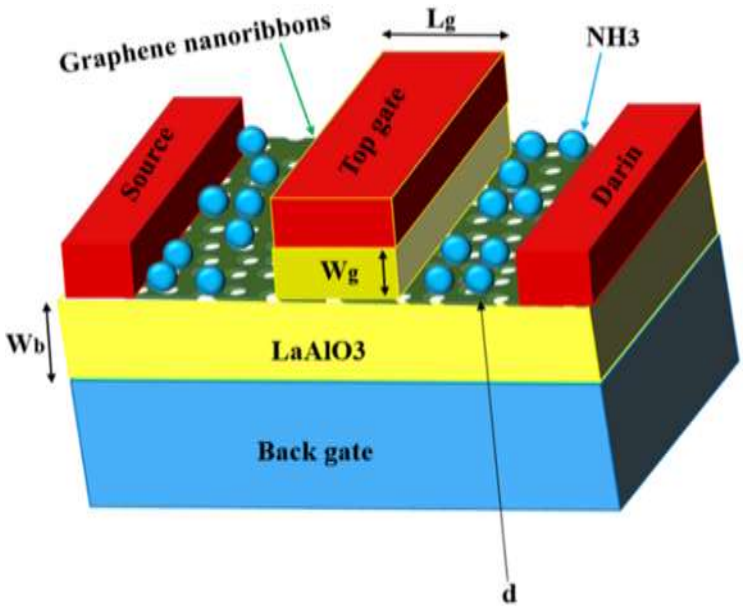


Figure V.1. *Structural schematic of the double gated graphene nanoribbon FET (DG-GNRFET) [17].*

In the proposed device configuration, the gate electrode is electrically separated from the graphene channel by a dielectric layer, while a silicon back gate is incorporated to modulate the carrier density or tailor the threshold voltage [1–3]. For applications demanding low power consumption and enhanced transconductance, lanthanum aluminate ($LaAlO_3$) is employed as

the high-k gate dielectric owing to its dielectric constant of approximately 30 and superior material properties. Compared to commonly used dielectrics such as hafnium oxide (HfO_2) and aluminum oxide (Al_2O_3), $LaAlO_3$ offers a higher-quality interface with graphene, significantly reducing charge trap densities that otherwise degrade sensor reliability and responsiveness. Moreover, $LaAlO_3$ demonstrates lower leakage currents, thus contributing to improved device stability and overall performance in graphene nanoribbon field-effect transistor (GNRFET) gas sensors [15].

Asymmetric double-gate configurations in graphene nanoribbon field-effect transistor (GNRFET) based gas sensors confer several critical advantages in device performance. By engineering differential thicknesses of the gate dielectric layers, the electrostatic control over the channel is significantly enhanced, which is especially beneficial in the subthreshold region where transistor sensitivity is paramount. The incorporation of a thicker gate oxide serves to suppress short-channel effects by effectively reducing leakage currents, thereby enhancing device stability and operational reliability. This architectural approach facilitates precise tailoring of the electric field distribution within the channel, enabling the optimization of sensor sensitivity and the acceleration of response dynamics. Consequently, such structural modulation permits the fine-tuning of sensor characteristics for the selective detection of various target gas species [16].

The detection of ammonia (NH_3) gas in the proposed device is realized by exposing the regions between the source and gate electrodes, as well as between the drain and gate electrodes, to the ambient environment. This deliberate exposure enables NH_3 molecules to adsorb onto the surface of the graphene nanoribbon channel. The adsorption process induces a modulation of charge carrier concentration in the graphene due to charge transfer interactions between the gas molecules and the channel. Consequently, these changes in carrier density directly affect the electrical properties of the device, manifesting as a measurable variation in the drain to source current (I_{ds}). This modulation of the drain current under NH_3 exposure constitutes the fundamental sensing mechanism, enabling the double gated graphene nanoribbon field-effect transistor (DG-GNRFET) to operate as an effective and sensitive gas sensor.

V.2 Current Analytical Model Overview for Double-Gated GNRFET Gas Sensor

In the present analysis, the channel electron population is treated as non-degenerate, an assumption that holds true under typical room temperature conditions and moderate doping levels characteristic of graphene nanoribbon field-effect transistors (GNRFETs). Nevertheless,

under scenarios involving increased doping concentrations or lower temperatures, carrier degeneracy can arise. Properly accounting for this degenerate regime is essential to improve the accuracy of device performance modeling and to ensure the model's applicability over a wider range of operational environments.

Accordingly, the electron and hole occupancy within the subbands near the source and drain regions are characterized by the following distribution functions [18]:

$$\varepsilon_{p,n}^{-1} = \pm v\sqrt{P^2 + (\pi\hbar/d)^2} \quad \text{(V-1)}$$

The device architecture employs a double-gate graphene nanoribbon field-effect transistor (GNRFET) featuring a narrow channel width of 2.06 nm, which theoretically corresponds to an energy bandgap of approximately 0.72 eV. It is important to recognize that this bandgap value is derived from an idealized, defect-free graphene nanoribbon (GNR) model. In practical device fabrication, however, the presence of edge roughness, atomic-scale defects, and structural variability is inevitable and can substantially impact the electronic characteristics of GNRs. Specifically, edge irregularities and lattice defects serve as scattering centers and introduce localized electronic states within the bandgap region. These imperfections can induce fluctuations in the effective bandgap, degrade carrier mobility, and contribute to performance variability manifested as decreased on/off current ratios and elevated noise levels. Such detrimental effects have been documented in multiple experimental studies, underscoring the challenges in achieving reproducible and high quality GNR-based devices.

To address these fabrication-induced limitations, advanced synthesis and patterning methodologies have been pursued. Bottom-up chemical synthesis techniques and high-resolution lithographic processes have demonstrated the capability to produce GNRs with improved edge smoothness and reduced defect densities, thereby enabling enhanced electronic performance. Considering these fabrication realities is essential for developing comprehensive device models and guiding the engineering of GNRFETs toward practical, high-performance applications.

The electronic transport is described by key parameters including the charge carrier velocity v=10^8 cm/s, the momentum along the graphene nanoribbon (P), and the reduced Planck constant ($\hbar$). This framework facilitates accurate modeling of the NH_3 gas sensing process by capturing the charge transfer interactions occurring at the graphene surface. The proposed model formulates the relationship between the device current, gas concentration, and temperature as expressed by equation (2):

$$I_{GAs-GNR} = I_{gT} + I_{gF} \qquad \text{(V-2)}$$

Where I_{wg} represents the baseline device current in the absence of gas exposure, encompassing the effects of intrinsic geometric and material parameters of the transistor. The term I_{gT} accounts for the variation in current arising from temperature-dependent effects, while I_{gF} denotes the modulation of the device current induced by changes in gas concentration at a fixed temperature. Specifically, I_{gF} quantifies the impact of gas molecule adsorption on the carrier density and transport characteristics within the graphene nanoribbon channel, thereby altering the conduction behavior of the sensor.

The conductivity of the gas sensor exhibits dependence on both ammonia (NH_3) concentration and operating temperature, consistent with observations reported in references [19,20]. In this configuration, the conventional top gate electrode is replaced by the active sensing region of the graphene nanoribbon field-effect transistor (GNRFET), geometrically defined by the spatial coordinates:

$$L_g/2 \leq x \leq L_g, \qquad 0 \leq z \leq W_b,$$

Here, L_g denotes the length of the top gate along the nanoribbon axis (x-direction, in nanometers), serving as a critical parameter influencing short-channel effects and carrier transport within the GNRFET. The parameter W_b represents the thickness of the dielectric layer separating the graphene channel from the back gate in the z-direction (nanometers), which plays a pivotal role in modulating the channel potential from beneath the substrate. The coordinate system is defined such that the x-axis aligns with the longitudinal direction of the graphene nanoribbons, while the z-axis is oriented perpendicular to both the nanoribbon plane and the gate electrode planes.

This spatial domain encompasses the active channel region subjected to electrostatic modulation by the gate potentials, thus governing the distribution of carriers and overall transport characteristics in the device. To analyze the electrostatic potential profile within the channel region, the two-dimensional Poisson equation is employed, and is formulated as follows [18]:

$$\frac{W_b+W_g}{3}\frac{\partial^2\varphi}{\partial x^2} - \frac{\varphi-V_b}{W_b} - \frac{\varphi-V_g}{W_g} = \frac{4\pi e}{æ}(\Sigma_- - \Sigma_+) \qquad \text{(V-3)}$$

Here, φ represents the electrostatic potential distribution along the channel. The quantities Σ_- and Σ_+ correspond to the electron and hole densities within the graphene channel,

respectively, reflecting the concentrations of negatively and positively charged carriers that contribute to electrical conduction.

e: Denotes the elementary charge of an electron, equal to 1.602×10^{-19} coulombs (C).

æ: Represents the dielectric permittivity of the material separating the graphene channel from the back gate.

W_g **:** Refers to the thickness of the insulating dielectric layer positioned between the graphene channel and the top gate,

V.3 Electrostatic Modeling and Boundary Conditions in GNRFET

In the simulations of the GNRFET device, the spatial distribution of the electrostatic potential within the graphene nanoribbon channel is determined by solving the two-dimensional Poisson equation.

$$\nabla \cdot (\varepsilon \nabla \varphi) = -\rho,$$

Where φ represents the electrostatic potential, ε denotes the dielectric permittivity, and ρ corresponds to the net charge density within the channel [21].

V.3.1 Lateral Edges of the Nanoribbon (Neumann Boundary Conditions)

The graphene nanoribbon regions in proximity to the source and drain terminals exhibit high conductivity and effectively function as ideal electron reservoirs. Consequently, the electrostatic potential at the channel boundaries adjacent to the source and drain contacts is fixed, thereby imposing Dirichlet boundary conditions expressed as:

Here, L_g denotes the gate length and V_d represent the applied drain voltage. This boundary condition maintains a consistent alignment of the electrostatic potential with the externally applied bias, thereby defining the Fermi levels at the source and drain contacts [22].

The segments of the graphene nanoribbon near the source and drain electrodes are highly conductive and effectively serve as stable electrical contacts. As a result, the electrostatic potential in these regions is fixed set to zero close to the source $\varphi = 0$ and equal to the applied drain voltage $\varphi = V_d$ at the drain end.

Lateral Edges of the Nanoribbon (Neumann Boundary Conditions)

At the sides of the graphene nanoribbon, the boundary condition assumes that there is no electric field component perpendicular to these edges. Mathematically, this is expressed by setting the normal derivative of the electrostatic potential to zero:

$$\left.\frac{\partial \phi}{\partial y}\right|_{\text{edges}} = 0,$$

which corresponds to the physicaW confinement and the lack of charge transport normal to the channel boundaries [22].

V.3.2 Gate Interfaces (Dirichlet or Mixed Boundary Conditions)

The dielectric layers associated with the top and back gates are held at constant potentials that match the applied gate voltages. These fixed potentials serve as boundary conditions at the dielectric interfaces, enabling precise electrostatic control over the channel potential [23].

V.3.3 Self-Consistent Determination of Charge Densities

The sheet charge densities of electrons (Σ^-) and holes (Σ^+) in the graphene nanoribbon channel are calculated in a self-consistent manner together with the electrostatic potential distribution. These charge densities are functions of the local electrostatic potential $\varphi(x, y)$as well as the Fermi levels at the source and drain contacts $E_{F,S}$ and $E_{F,D}$, which are controlled by the respective applied voltages. More specifically, the values of $\Sigma^-$and Σ^+ are obtained by integrating the graphene nanoribbon's density of states multiplied by the Fermi-Dirac occupation probabilities across the energy spectrum.

$$\Sigma^{\pm}(x, y) = \int D(E) f(E - E_F(x, y)) dE,$$

Where *D(E)* represents the density of states of the graphene nanoribbon as a function of energy, indicating the number of electronic states available per energy interval at energy *E*.

$$E_F(x, y) = E_{F,\text{contact}} - q\varphi(x, y)$$

This term incorporates the effect of local band bending arising from variations in the electrostatic potential, which influences the energy landscape and charge carrier distribution within the device [22,24].

V.3.4 Electrostatics Near the Contacts

At the interfaces between the metal contacts and the graphene nanoribbon, the Fermi levels are firmly established, while the electrostatic potential is governed by the applied bias voltage. Carrier injection and extraction processes are simulated by applying the boundary potentials as previously outlined. The charge density undergoes a rapid change close to the contacts, in agreement with quantum transport modeling, thus providing an accurate description of the electrostatics at the device contacts [22].

Equation (3) describes the spatial distribution of the electric potential within the device. This framework allows for a detailed analytical investigation of the non-uniform potential variations along the GNRFET channel and supports a thorough evaluation of short-channel effects. The electron densities at the source and drain regions are directly connected to the Fermi levels, local electrostatic potential, and essential physical constants as expressed by the following relations: $\Sigma_{\pm}^{S} = \frac{2\sqrt{2\Delta K_B T}}{\sqrt{\pi}\hbar d\nu} exp\left(\pm\frac{\varepsilon_f^S + e\varphi}{K_B T} - \frac{\Delta}{2}K_B T\right)$,

$$\Sigma_{\pm}^{D} = \frac{2\sqrt{2\Delta K_B T}}{\sqrt{\pi}\hbar d\nu} exp\left(\pm\frac{\varepsilon_f^D + e(\varphi - V_d)}{K_B T} - \frac{\Delta}{2}K_B T\right) \quad \text{(V-4)}$$

Table V.1. *Electrical Parameters of the GNRFET Structure*

Parameter	Description
$\Sigma_{\pm}^{S}, \Sigma_{\pm}^{D}$	The electron densities (electron/hole flux) at source/drain contacts [cm^{-2}]
$\varepsilon_f^S, \varepsilon_f^D$	Fermi energy levels at source/drain contacts
φ	Electrostatic potential in the channel [V]
V_d	Drain voltage bias[V]
Δ	Energy bandgap of graphene nanoribbon [eV]
ν	Carrier velocity or attempt frequency [cm/s]
K_b	Boltzmann constant [m2kgs-2K-1]
$\hbar$	The reduced Planck constant
e	Elementary charge [Coulombs]
T	Absolute Temperature [Kelvin (K)

The energy bandgap is given by the expression $\Delta = 4\pi\hbar/d$, where the terms have their usual physical meanings. Assuming that the charge transport is primarily controlled by the potential barrier at the interface between the electrodes and the graphene nanoribbon (GNR), the current per unit channel length can be described by the following equation [18]:

$$I_{wg} = \frac{2e}{\pi\hbar d}\left(\int v_p f_p^S dp - \int v_p f_p^D dp\right) \quad \text{(V-5)}$$

Here:

$$v_p = \frac{d\varepsilon_{p,0}^{+}}{dP} = v^2 \frac{P}{\sqrt{v^2P^2+\Delta^2/4}} \quad \text{(V-6)}$$

v_p : represents the electron velocity associated with momentum p in the conduction band of the graphene nanoribbon. The distribution functions f_p^d and f_p^s correspond to the Fermi-Dirac occupation probabilities at the source and drain contacts, with their Fermi energies referenced relative to the mid-gap energy level. Direct integration of Equation (V-5) yields the result shown in reference [18].

$$I_{wg} \propto \begin{cases} \frac{Vgs+\frac{Vb.Wg}{Wb}}{Wb+Wg} \cdot \left(1 - \frac{1}{coshcosh\left(\frac{Lg}{2\Lambda}\right)}\right) + \frac{Vd}{2coshcosh\left(\frac{Lg}{2N}\right)}; & at\ |V_g| > V_bWg\ /\ Wb \\ \frac{Vgs.Wb}{Wb+Wg} \cdot \left(1 - \frac{1}{cosh\left(\frac{Lg}{2\Lambda}\right)}\right) \cdot \left(1 + \frac{Wb}{Wb+Wg} \cdot \frac{1}{e.\frac{Vb}{K_b.T}}\right); & at\ |V_g| \leq VbWg\ /\ Wb \end{cases} \quad \text{(V-7)}$$

In this context $\Lambda = \sqrt{(W_b/3)}$ represents the effective screening length.

V.4. Current with Gas Exposure

The parameters IgT and IgF related to gas exposure can be linked and expressed as a single combined parameter, as detailed in reference [25].

$$I_{Gas} = I_{gT} + I_{gF} = \frac{2e}{\pi\hbar d}\left(\int \left(\frac{x^{-2}}{1+e^{x-\eta}}dx + \frac{x^{-2}}{1+e^{x+\eta}}dx\right)\right) \quad \text{(V-8)}$$

Here, $\eta = (E_F - E_G)/k_BT$ and $x = (E - E_G)/k_BT$ represent the normalized Fermi energy values. The numerical solution of this equation is carried out using the method of partial integration [20, 26], sequently, the general current model for this graphene-based gas sensor component can be developed in a manner analogous to the silicon-based model proposed by Gunlycke et al. [27].

$$I_{Gas} = \frac{2e}{\pi\hbar d}\left(\xi_{-1/2}\frac{E_F-E_G}{K_BT} + \xi_{-1/2}\frac{E_G-E_F}{K_BT}\right)V_{gs} \quad \text{(V-9)}$$

The Fermi-Dirac integral of order (−1/2), denoted as $\xi-1/2$, plays a fundamental role in the theoretical modeling of semiconductor properties. The bandgap energy (E_G) critically affects the conductance of the gas sensor, as it is dependent on both the concentration of the gas and the operating temperature [19]. This dependency can be formally expressed as follows [28]:

$$E_G = \delta T + \lambda F$$

The parameter δ used to describe how the energy bandgap responds to changes in temperature, reflecting its temperature sensitivity. The parameter λ accounts for the variation in the energy bandgap resulting from gas adsorption, effectively monitoring gas concentration. Additionally, F represents the gas concentration, measuring the amount of gas interacting with the graphene nanoribbon. These parameters collectively define how the energy bandgap depends on both temperature and gas concentration. Their initial definitions and derivations originate from earlier investigations of Carbon Nanotube Field Effect Transistors (CNTFETs), which share comparable physical mechanisms with graphene nanoribbon FETs (GNRFETs). An illustrative case is the semi-empirical modeling framework developed by Marani and Perri (2017) [29], which integrates the temperature dependence of the energy bandgap into the current-voltage (I–V) characteristics of Carbon Nanotube Field Effect Transistors (CNTFETs). The parameters within this model are obtained through an iterative computational method [30].

The current model for the gas sensor, derived from Equations (9) and (10), can be expressed as follows:

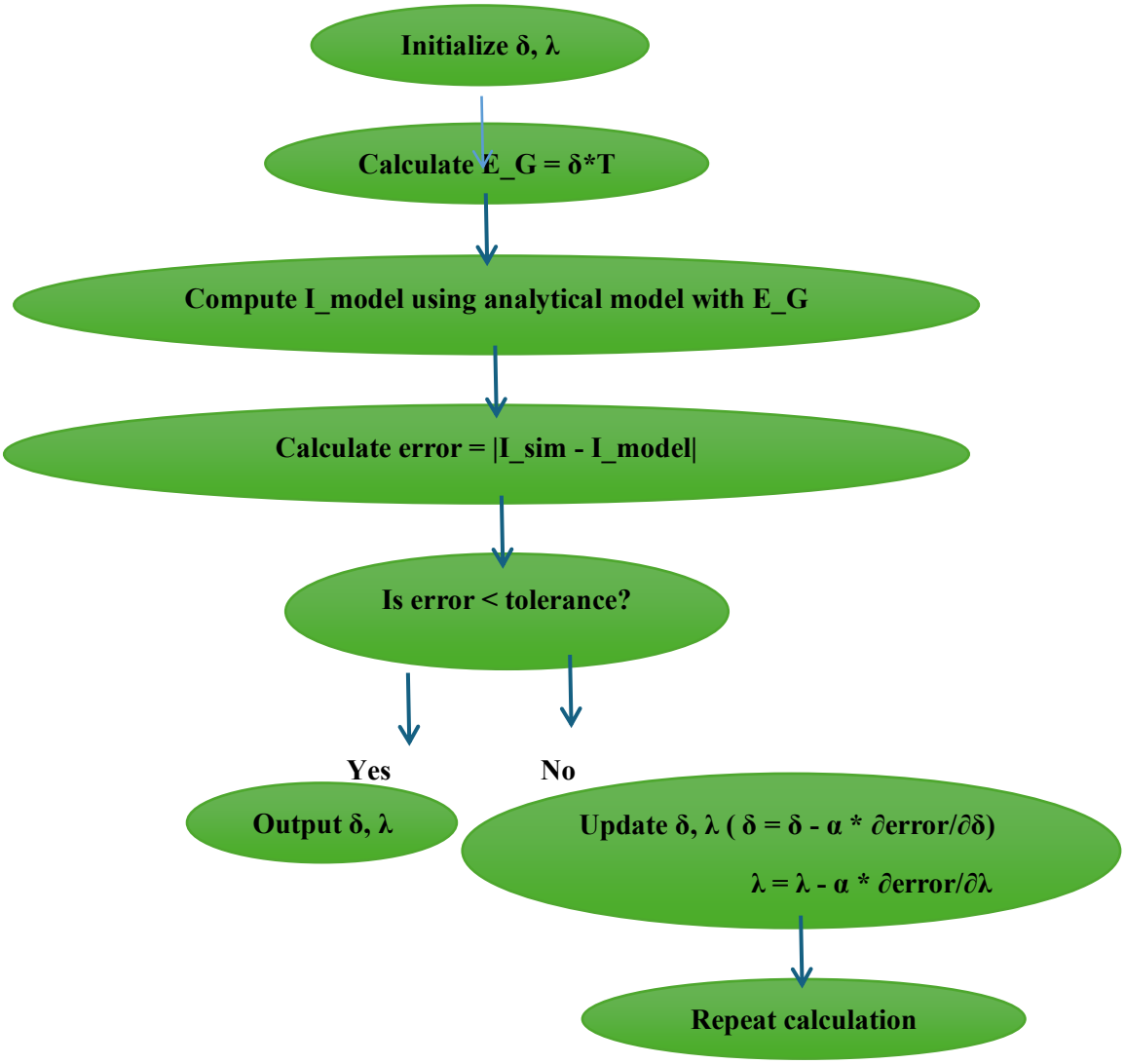
$$I_{Gas} = \frac{2e}{\pi\hbar d}\left(\xi_{-1/2}\frac{E_F-(\delta T+\lambda F)}{K_B T} + \xi_{-1/2}\frac{(\delta T+\lambda F)-E_F}{K_B T}\right)V_{gs} \qquad \text{(V-10)}$$

By integrating equations (7) and (10) along with the pertinent relations, a comprehensive formula for the source-drain current is obtained, which depends on the top gate voltage, channel length, gas concentration, and temperature. This detailed formulation facilitates an in-depth evaluation of the performance of the graphene-based gas sensor field-effect transistor (FET) under various operational conditions, providing critical insights into the impact of key parameters on the sensor's efficiency and responsiveness.

$$I_{Gas-GNR} = v\left(\frac{æ}{2\pi^{3/2}.Wb}\right)\left(\sqrt{\frac{K_B.T}{\delta}}\,exp\left(\frac{e.\varphi_m}{K_B.T}\right)V_b - (V_b - V_{ds})exp\left(-\frac{e.Vds}{K_B.T}\right) - \left(\frac{6q^2}{\hbar Lg}\right)(3a_{cc}tK_BT)^{1/2}\left(\frac{2}{\sqrt{\pi}}\sqrt{\frac{E_F-E_G}{K_BT}}\left(\frac{E_F-E_G}{K_B\cdot T}\right) + \frac{2}{\sqrt{\pi}}\sqrt{\frac{-E_F+E_G}{K_BT}}\left(\frac{E_F-E_G}{K_B\cdot T}\right)\right)(V_{gs}-V_{th})\right) \qquad \text{(V-11)}$$

Performance evaluation of graphene-based gas sensor field-effect transistor (FET) devices is conducted using a particular equation derived from their current-voltage (I–V) behavior. The variation in top gate voltage, induced by gas exposure, serves as a control mechanism for the drain-source current. Our model operates similarly to traditional MOSFET devices, encompassing both the ohmic and saturation regions. This approach underscores the adaptability of graphene as a material to enhance gas sensor performance. Nevertheless, the assumption of a non-degenerate electron gas, although simplifying the analysis of GNRFET-based gas sensors, may not comprehensively represent the intricate electronic properties of graphene across all operating conditions.

V.5 Flowchart of the Iterative Extraction Process



This model demonstrates inherent limitations when applied to scenarios involving high doping concentrations and low temperature conditions. However, it retains validity and yields reliable predictions for GNRFET operation at ambient temperatures with moderate doping, where the electron gas can be justifiably approximated as non-degenerate. This approximation facilitates more tractable analytical and computational modeling, allowing for the extraction of meaningful insights into overall behavioral trends without incurring significant computational demands. Consequently, although this assumption simplifies the analysis, its constraints under conditions of elevated doping or reduced temperatures must be carefully acknowledged to ensure accurate performance characterization [31–33].

Simulation Framework and Numerical Implementation: The electrostatic potential distribution was determined by solving the two-dimensional Poisson equation via the finite difference method (FDM) applied on a uniform spatial grid. To enhance convergence rates, the iterative Successive Over-Relaxation (SOR) method was utilized, with the relaxation parameter optimally set at approximately 1.8. Numerical precision was ensured by enforcing a convergence threshold defined by a relative residual below 10^{-6}. Given that the simulations address steady-state conditions, temporal integration was not required. All computational simulations were conducted using MATLAB R2023a. The framework primarily leveraged built-in MATLAB functions, obviating the need for specialized toolboxes. Custom scripts were developed for tasks including discretization, matrix assembly, and the iterative resolution of the governing equations.

The boundary conditions were meticulously applied as follows: Dirichlet conditions were used to set the electrostatic potential at the source and drain terminals according to the applied bias voltages. The gate voltage was modeled by imposing a fixed potential at the gate dielectric interface. Along the lateral boundaries of the simulation domain, Neumann conditions with zero normal derivative were enforced to simulate insulating barriers and ensure the preservation of charge neutrality. These boundary conditions are consistent with established methodologies in quantum transport simulations of graphene nanoribbon field-effect transistors (GNRFETs).

A uniform mesh grid featuring a spatial discretization of 0.1 nm was utilized along both the channel length and width dimensions. This high-resolution mesh was chosen to precisely resolve quantum confinement phenomena and the spatial variations in electrostatic potential within the graphene nanoribbon channel.A uniform mesh grid with a spatial discretization of

0.1 nm along both the channel length and width was employed. This fine mesh resolution was selected to accurately capture quantum confinement effects and potential variations within the graphene nanoribbon channel.

V.6 Results and Discussion

This section details the simulation outcomes for the graphene nanoribbon field-effect transistor (GNRFET). A comprehensive analysis of the current-voltage (I–V) characteristics is conducted to investigate the influence of pivotal parameters on the device's performance. The results provide essential understanding of the GNRFET's operational dynamics under different conditions, highlighting its significant potential for applications in gas sensing and other related technological fields.

Table V.2. *Key Parameters for the Proposed Device Design.*

Device parameters	**Value**
Graphene Nanoribbon (GNR) Type	armchair
GNR band gap energy	0.72 eV
Graphene channel width	2.06 nm
Gate length (L_g)	100 nm
Top Gate Dielectric Thickness (W_g)	30 nm
Back Gate Dielectric Thickness (W_b)	70 nm
Dielectric constant (k)	30
Temperature (T)	300

Figure V.**2.** depicts the current-voltage (I-V) responses of a simulated graphene nanoribbon field-effect transistor (GNRFET) device with defined dimensions gate length $L_g = 100\text{nm}$, gate width $W_g = 30\text{nm}$, and base width $W_b = 70\text{nm}$ recorded both in the absence and presence of ammonia (NH_3) gas. The measurements were taken under various gate bias conditions ($V_{gs} = 0.72, 0.74, 0.76, 0.74,$ and 0.80V). The transistor exhibits conventional FET behavior, where the drain current (I_{ds}) increases with increasing drain voltage (V_{ds}) until reaching a saturation point at elevated voltage levels. Additionally, an increase in gate voltage corresponds with a higher drain current, reflecting improved conduction through the graphene channel. Exposure to NH_3 at 300 ppm results in a pronounced increase in the drain current across all gate voltages tested.

This effect arises from the electron-donating property of NH_3, which leads to an increase in electron density within the graphene channel region. Consequently, this rise in carrier concentration enhances the device's conductivity, producing a significant increase in drain current rising from approximately 10^{-7} A to 10^{-5} A. These findings confirm the effectiveness of GNRFET devices as sensitive and reliable NH_3 gas sensors. The marked escalation in drain current detected upon NH_3 gas exposure quantitatively highlights the exceptional sensitivity of the GNRFET, affirming its ability to accurately detect even minimal fluctuations in ambient NH_3 levels. Such a pronounced response firmly establishes the GNRFET as a highly promising technology for sophisticated gas sensing applications, particularly within vital sectors including environmental monitoring, industrial process regulation, and cutting-edge safety frameworks. Similar findings have been consistently documented in previous research [34, 35].

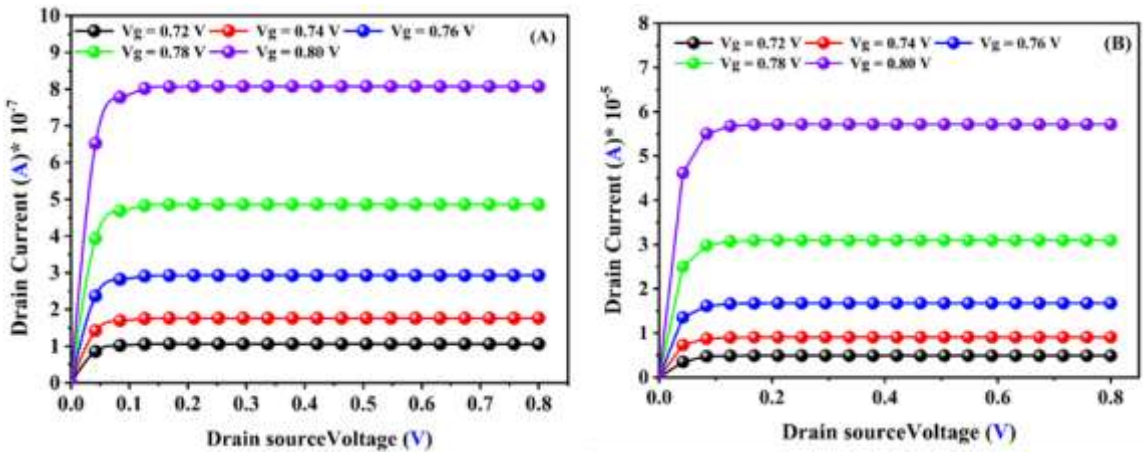


***Figure** V.2. Current-voltage (I-V) characteristics: (a) measured in the absence of NH_3, and (b) measured after exposure to NH3 at a concentration of 300 ppm.*

The sensitivity of the graphene nanoribbon field-effect transistor (GNRFET) is rigorously defined as the percentage variation in current in response to exposure to the target gas, and is quantitatively determined using the following equation:

$$S = \frac{(Ig - Iwg) \times 100}{Iwg} \qquad \text{(V-12)}$$

In this context, Ig represents the drain current recorded during gas exposure, while Iwg denotes the baseline drain current measured in the absence of the gas. This formulation offers a normalized and intuitive metric for evaluating sensor performance and aligns with established

methodologies frequently employed in graphene- and carbon nanotube-based sensor research [36–38]. Sensitivity is represented as a normalized variation in an electrical parameter, enabling direct comparison among diverse sensor platforms. As illustrated in **Figure V.3**, the data reveal that exposure to 450 ppm NH_3 results in a sensitivity enhancement of 120% at a gate voltage (V_g) of 0.8 V and a temperature of 300 K.

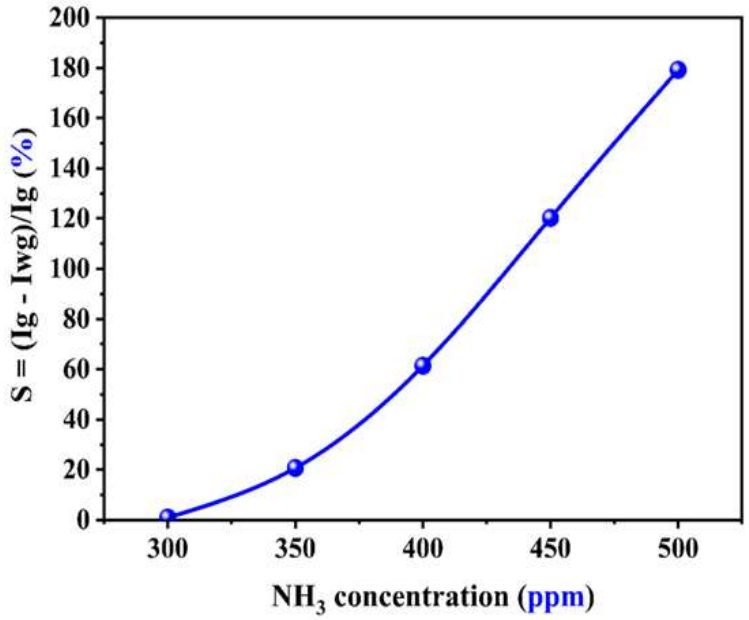


Figure V. 3. *Influence of NH_3 concentration on sensor sensitivity.*

The sensor's sensitivity exhibits an approximately linear response, likely due to the pronounced modulation of the Schottky junctions formed at the interface between the graphene nanoribbon and the electrodes.

Our sensor design notably achieves a sensitivity near 120% at 450 ppm, which significantly exceeds that of conventional GNRFET gas sensors reporting only 55% sensitivity at the same concentration, thereby demonstrating improved detection capability for NH_3. Moreover, the CNT/rGO-Am sensor also shows high sensitivity toward NH_3. This comparison emphasizes the advantage of utilizing nanomaterial-based sensors for applications requiring elevated sensitivity.

Table V.3*.Sensitivity comparison of our GNRFET gas sensors against other comparable configurations.*

Sensor Type	Gas Type	Concentration	Sensitivity %	Reference
GNRFET gas sensor	NH_3	450 ppm	120 %	Our model
GNRFET	NH_3	1 ppm	2.7 %	[35]
GNRFET	NH_3	450 ppm	55 %	[35]
CNT/ rGO-Am sensor	NH_3	400 ppm	115 %	[39]

Figure V.4. presents the current-voltage (I–V) characteristics of the GNRFET device measured at room temperature (300 K) under a fixed gate voltage of 0.7 V, exposed to varying ammonia (NH_3) concentrations (300, 350, 400, 450, and 500 ppm). The findings reveal a distinct and concentration-dependent increase in drain current with NH_3 exposure, indicating enhanced charge carrier modulation within the graphene nanoribbon channel. This pronounced effect demonstrates the device's exceptional sensitivity and effective signal transduction for NH_3 detection, driven by charge transfer interactions that influence the channel's conductivity. These results validate the GNRFET as a highly promising candidate for selective and sensitive gas sensing applications. The observed enhancement in performance is primarily due to NH_3 acting as an electron donor, which raises the electron concentration in the n-type graphene nanoribbon. As the NH_3 concentration increases, more electrons are injected into the channel, thereby boosting its conductivity and modulating the transistor's electrical response. As a result, the elevated charge carrier density causes a significant rise in the drain current (I_{ds}), illustrating the effect of chemical doping induced by the interaction with gas molecules [40].

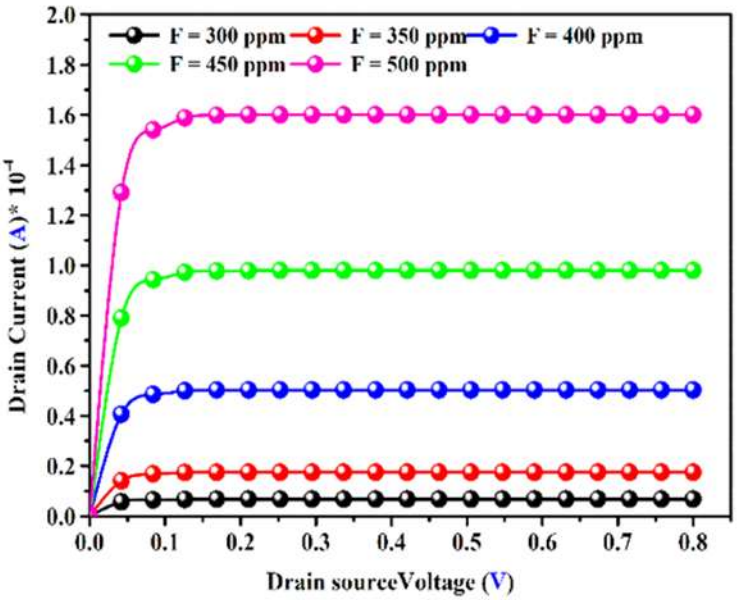


Figure V.4. *presents the drain current (I_{ds}) versus drain-source voltage (V_{ds}) characteristics of the GNRFET transistor measured at different NH_3 gas concentrations, conducted at room temperature (T = 300 K).*

The findings clearly indicate that the GNRFET transistor responds robustly and reproducibly to variations in NH_3 gas concentration, as demonstrated by the quantifiable changes in the drain current. This pronounced sensitivity across the investigated concentration range underscores the transistor's effectiveness in NH_3 detection, affirming its strong potential for deployment in environmental monitoring and gas sensing applications. The observed modulation of current with increasing NH_3 levels validates the device's capability for reliable and sensitive gas detection. The present investigation concentrates on NH_3 concentrations between 300 and 500 ppm, a range strategically chosen to elucidate the fundamental charge transfer and transport phenomena governing the device's response.

This concentration window corresponds with previous theoretical and simulation studies, such as those conducted by Tamersit et al. [34], Mahmoudi et al. [35], facilitating direct comparison and corroboration of the results. Although detection at lower concentrations particularly at parts-per-billion (ppb) levels is critical for numerous practical applications, modeling sensor performance under such conditions presents additional challenges. These challenges include weak physisorption effects, stochastic adsorption-desorption kinetics, and intrinsic device noise, necessitating advanced multi-scale modeling approaches that exceed the scope of the present study. Future research will aim to extend the simulation framework to incorporate these complex phenomena, thereby enabling a comprehensive exploration of the

sensor's detection limits and sensitivity at sub-ppm NH_3 concentrations. Such progress will significantly enhance the practical viability of GNRFET-based gas sensors in real world detection scenarios.

This establishes GNRFET as a highly effective platform for real time NH_3 monitoring, vital for diverse sectors such as agriculture and environmental science [41]. However, it is important to recognize that prolonged ammonia exposure can negatively impact the long term stability and structural integrity of GNRFET sensors due to strong adsorption effects, extended recovery periods, irreversible alterations in electrical characteristics, and possible mechanical degradation. Consequently, continued research into passivation strategies and material enhancements is critical to bolster the durability and reliability of these sensors for practical, real-world deployment [42, 43].

Figure V.5. presents the current-voltage (I-V) characteristics measured at room temperature for different back gate voltages (V_b = 1, 2, and 3 V) under an ammonia (NH_3) concentration of 300 ppm. The results demonstrate a consistent pattern in which the source-drain current (I_{ds}) increases with rising drain voltage (V_{ds}) across all back gate voltage values. This behavior is primarily due to the increased electron density within the graphene channel, driven by the back gate voltage. By modulating the electrostatic potential, higher back gate voltages augment the charge carrier concentration in the channel. Consequently, the elevated electron density enables a greater current flow under an applied drain voltage, indicating a direct and positive relationship between the drain current and the back gate voltage. The gate-dependent response patterns reveal a fundamental distinction between electrostatic modulation and sensitivity driven by adsorption.

As illustrated in **Figure** V.**5.** applying back gate voltage (V_b) increases baseline conductivity by broadly tuning the carrier density, yet it exerts little influence on sensitivity because the mechanisms governing gate electrostatics and gas adsorption are inherently different. The back gate chiefly adjusts the overall electrostatic potential within the channel, while sensitivity to NH_3 arises from localized interactions on the graphene surface exposed to the gas. Therefore, the uniform electrostatic effect of V_b does not affect the efficiency of charge transfer for each adsorbed molecule, leading to a stable relative current response across various back gate voltages. In contrast, the top gate, despite its strong electrostatic control, is encapsulated, preventing it from interacting with gas adsorption processes. This mechanistic

separation highlights that enhancing sensor sensitivity is primarily dependent on surface modification rather than gate voltage manipulation.

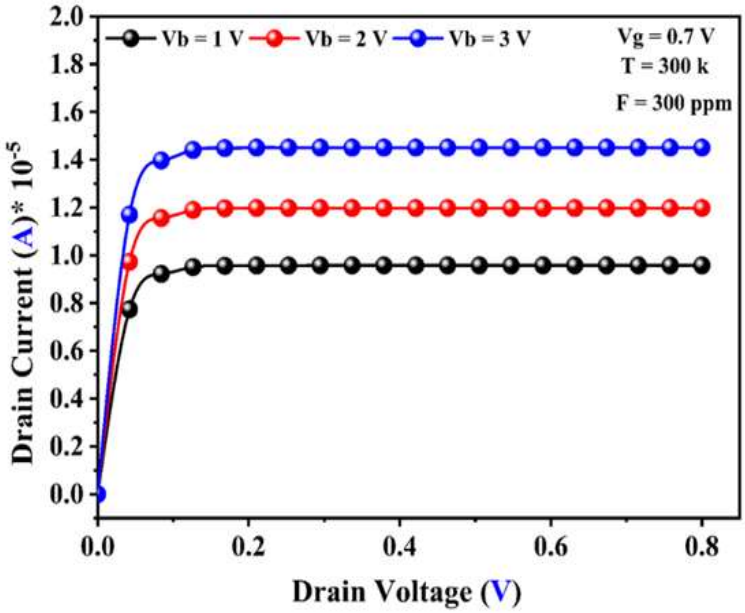


***Figure** V.5. Current-voltage (I-V) characteristics measured at varying back gate voltage levels.*

These findings are consistent with previous research highlighting the effectiveness of graphene nanoribbon field-effect transistors (GNRFETs) as highly sensitive gas detectors, particularly for ammonia (NH_3). For instance, a sensitivity of around 2.7% has been documented upon exposure to 1 ppm NH_3 [35], these observations emphasize the ability of GNRFETs to convert gas adsorption phenomena into quantifiable electrical responses. The observed sensitivity arises from charge transfer interactions between NH_3 molecules and the graphene nanoribbon channel, which alter the device's conductance. While the back gate exerts a limited effect on sensitivity, operating the GNRFET within the subthreshold region can improve detection capabilities. Overall, these results demonstrate the strong potential of GNRFET-based designs for developing low-power, highly sensitive gas sensors. **Table.V.3** Sensitivity comparison of our GNRFET gas sensors against other comparable configurations.

Earlier studies have greatly advanced the understanding of the relationship between gate voltage and current in field-effect transistors (FETs). Nonetheless, the impact of the insulating layer thickness separating graphene from the gate electrodes namely the top gate (W_g) and back gate (W_b) has often been overlooked. This aspect is crucial, as the properties of the dielectric

layer play a key role in the electrostatic control of the channel, which directly influences the drain current (I_{ds}) **Figure** V.**6** fills this gap by illustrating the variation in drain current (I_{ds}) with respect to drain voltage (V_{ds}). Panel (a) investigates how the thickness of the insulating layer between graphene and the top gate affects device performance, while panel (b) explores the corresponding effect of the layer thickness between graphene and the back gate. These measurements were conducted under continuous exposure to NH_3 gas at a concentration of 300 ppm and at room temperature (T = 300 K), offering a realistic context to assess the sensor's operational gas-sensing capabilities.

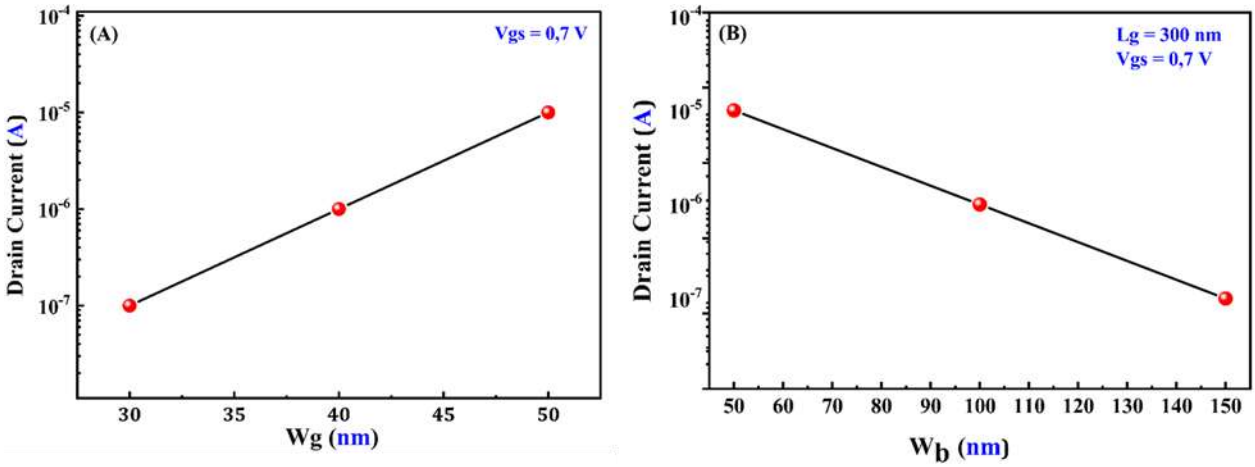


***Figure** V.**6**. Variation of the drain current (I_{ds}) versus drain-source voltage (V_{ds}) for different thicknesses of the insulating layer between graphene and (a) the top gate and (b) the back gate.*

As the thickness of the back gate insulating layer increases, the drain-source current (I_{ds}) correspondingly rises. This phenomenon is attributed to the enhanced capacitance associated with a thicker dielectric, which strengthens the electrostatic coupling between the back gate and the graphene channel. Improved coupling facilitates more effective modulation of charge carrier density in the graphene, thereby increasing the current flow. In contrast, an increase in the top gate insulation thickness causes a reduction in Ids, indicating that a thicker dielectric weakens the top gate's electrostatic control over the graphene channel. As a result, the gate voltage's ability to regulate the carrier concentration diminishes with greater insulation thickness, leading to decreased current conduction. This inverse correlation highlights the critical role of gate architecture and material properties in maximizing device performance. Additionally, the study investigated the impact of various parameters on the I_{on}/I_{off} ratio.

The influence of gate length on the I_{on}/I_{off} ratio is examined, as depicted in **Figure V.7**. The study focuses on a Graphene Nanoribbon Field-Effect Transistor (GNRFET) with a

permittivity (k) of 30, a body width (W_b) of 70 nm, and a gate width (W_g) of 20 nm, operated at 300 K. The back gate voltage (V_b) is tested at two values, 0.3 V and 0.7 V, while the drain voltage (V_{ds}) is held constant at 0.4 V. The top gate voltage varies between 0.72 V and 1.0 V. From the results shown in Figure V.7**,** it is evident that current density inversely correlates with back gate voltage for fixed channel lengths: increasing the back gate voltage leads to a reduction in current density. This trend is likely due to stronger electrostatic control exerted by the gate, which alters carrier density and mobility. Additionally, at a given back gate voltage, current density declines as the channel length increases. This inverse relationship underscores the critical role of gate length in device behavior, where longer channels contribute to greater resistance and, consequently, lower current conduction.

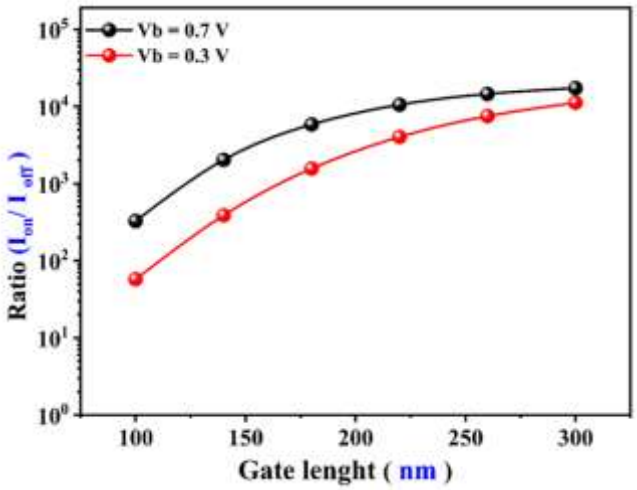


Figure V.7. *Dependence of the I_{on}/I_{off} ratio on the gate length.*

Figure V.**8**. depicts the variation of the I_{on}/I_{off} ratio as a function of the back-gate voltage (V_b) in the graphene nanoribbon field-effect transistor (GNRFET) gas sensor. In this study, the back gate voltage was systematically varied across values of 0.3 V, 0.5 V, 0.7 V, 0.9 V, and 1.0 V, while the drain-source voltage (V_{ds}) was held constant at 0.4 V. This range was selected to thoroughly examine how back gate bias influences device behavior, particularly in terms of channel conductivity modulation and the resulting I_{on}/I_{off} ratio. By analyzing multiple back gate voltages at a fixed V_{ds}, the electrostatic control exerted by the back gate under realistic operating conditions was comprehensively characterized. The results demonstrate a marked increase in the I_{on}/I_{off} ratio with higher V_b values, which is attributed to enhanced electrostatic regulation of the channel potential. As V_b rises, the gate-induced electric field more effectively adjusts the carrier concentration within the graphene nanoribbon, leading to a shift in the Fermi level and corresponding changes in channel conductivity.

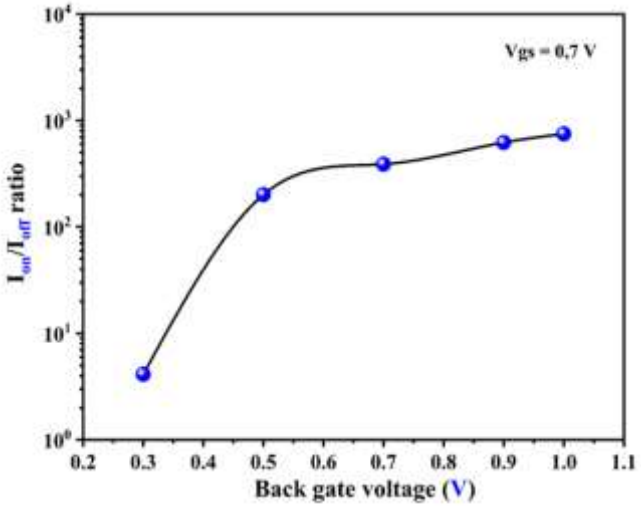


***Figure** V.8. Dependence of the I_{on}/I_{off} ratio on the back-gate voltage (V_b).*

Specifically, the off-state current (I_{off}) diminishes as a result of more effective carrier depletion, which elevates the potential barrier and mitigates leakage currents. Simultaneously, the on-state current (I_{on}) rises due to the channel's enhanced conductivity under elevated gate bias, promoting more efficient carrier injection and transport. The synergistic effect of these phenomena diminished I_{off} coupled with augmented I_{on} yields a significant enhancement in the I_{on}/I_{off} ratio, a parameter crucial for attaining both high sensor sensitivity and low power consumption. This observed behavior aligns with established theoretical and empirical research on GNRFETs, where improved electrostatic control through back-gate biasing enhances switching performance and amplifies the sensor's responsiveness to adsorbed gas molecules. The augmented I_{on}/I_{off} ratio at increased back-gate voltages thereby not only signifies superior device operation but also elevates detection efficacy by improving the signal-to-noise ratio in the presence of target gas analytes.

Figure V.**9.** (*a* and *b*) illustrate the dependence of the on-state current (I_{on}) and the I_{on}/I_{off} ratio on gate dielectric permittivity across three different temperatures (T = 200, 300, and 400 K). The Ion measurements were conducted at a gate-source voltage (V_{gs}) of 0.7 V and a drain-source voltage (V_{ds}) of 0.4 V, whereas I_{off} was determined at V_{gs} = 0 V and V_{ds} = 0.4 V. An increase in gate dielectric permittivity is associated with a corresponding rise in the I_{on}/I_{off} ratio. This behavior is primarily attributed to enhanced electrostatic coupling between the gate and the channel, which improves gate control and facilitates more effective modulation of the device current. Specifically, materials with higher permittivity strengthen this coupling, resulting in an elevated Ion relative to I_{off}. Additionally, temperature plays a significant role in influencing both the dielectric properties of the gate material and the I_{on}/I_{off} ratio. As

temperature increases, modifications in the dielectric characteristics contribute to a further enhancement of the I_{on}/I_{off} ratio, underscoring the importance of thermal effects in optimizing transistor performance. This highlights the need to carefully tailor device parameters for different operating temperatures. Notably, temperature impacts the performance of CNTFET transistors differently when no NH_3 is present [44].

At higher temperatures, thermal energy promotes the transfer of charge carriers between gas molecules and the GNRFET. When gas molecules adsorb onto the graphene surface, they can donate electrons to the device, modifying its conductivity and increasing the drain current, which in turn enhances the sensor's sensitivity. The current simulations focus on intrinsic graphene nanoribbons operating close to room temperature, making the non-degenerate electron gas approximation suitable and consistent with the physical conditions examined. The model utilizes a self-consistent solution of the two-dimensional Poisson equation coupled with carrier transport equations, allowing for an accurate representation of the spatial distribution of electrostatic potential and charge density within the channel. This methodology inherently captures the electrostatic behavior without explicitly accounting for electron degeneracy effects. Although appropriate for the moderate doping levels and temperature range considered, scenarios involving higher doping concentrations or lower temperatures would require the incorporation of Fermi–Dirac statistics to accurately describe degenerate carrier behavior. Future research will aim to extend the model to cover these regimes, thereby expanding its applicability. Clearly stating these assumptions helps delineate the model's scope and its inherent limitations.

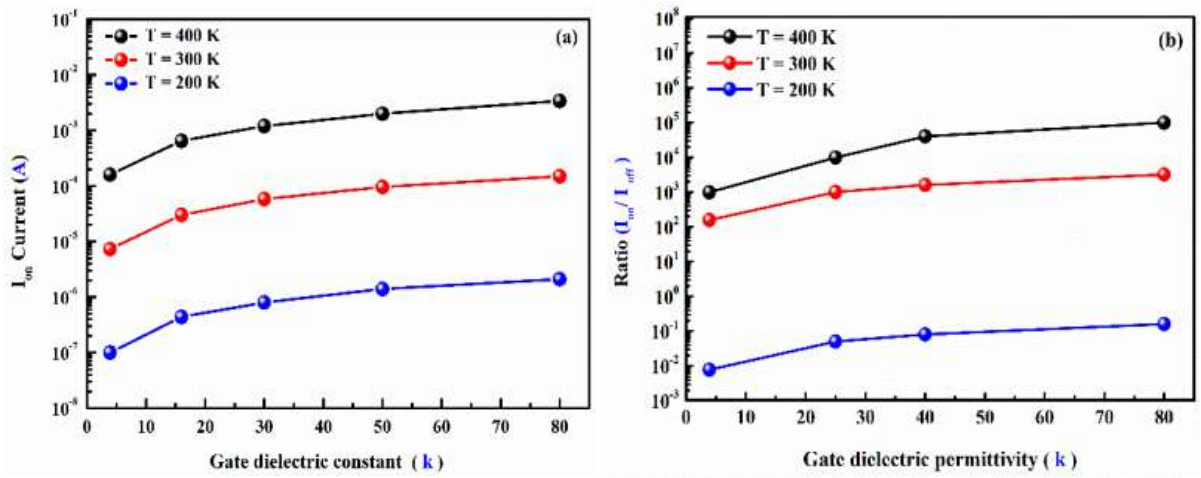


***Figure** V.9. (a) Change in Ion with respect to gate dielectric permittivity, (b) change in I_{on}/I_{off} ratio as a function of gate dielectric permittivity.*

Figure V.**10.** depicts the change in drain current density relative to gate length, focusing on two distinct top gate thicknesses (W_g = 10 nm and 20 nm) for both the ON state (Ion) in panel (a) and the OFF state (I_{off}) in panel (b). The data clearly show an exponential decline in drain current density (J_d) as gate length increases. Specifically, at gate lengths of 50 nm, 70 nm, and 100 nm, the current densities are approximately 3×10^{3} mA/cm², 4×10^{-1} mA/cm², and 3×10^{-3} mA/cm², respectively. This pattern reveals a strong inverse relationship between current density and gate length, indicating that longer gate lengths correspond to a substantial reduction in current density. **Figure** V.**10** shows that increasing the thickness of the insulating layer between graphene and the gate electrode leads to a rise in current density, highlighting a direct relationship between the layer thickness and the device's current performance. Specifically, for a gate width (W_g) of 20 nm, the current density (J_d) is higher compared to that at W_g = 10 nm. The carrier density, defined as the number of charge carriers per unit area in the transistor, increases with gate width because a wider gate facilitates the flow of more charge carriers through the channel. This elevated carrier density results in a higher drain current and enhanced current density. In contrast to the effect of gate length on current density where an increase in gate length causes a reduction in current density the relationship between gate length and the ON/OFF current ratio (I_{on}/I_{off}) follows an opposite trend.

As shown in **Figure** V.**10** longer gate lengths improve the I_{on}/I_{off} ratio. For example, at a gate length (L_g) of 50 nm, the I_{on}/I_{off} ratio is approximately 10^3 for a gate width of 10 nm, while it rises significantly to 3×10^2 for a gate width of 20 nm. This finding suggests that optimizing gate length is an effective strategy to enhance the device's switching capabilities by

increasing the I_{on}/I_{off} ratio, which is essential for achieving superior performance in practical applications.

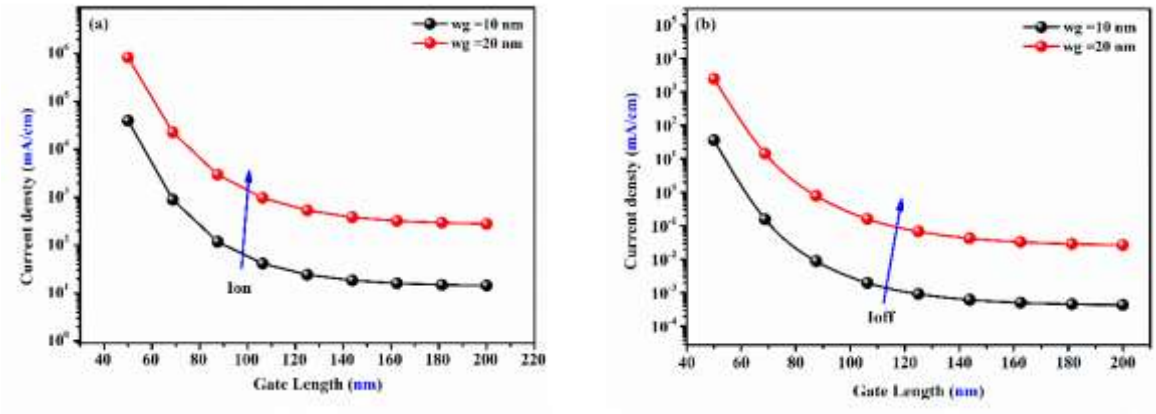


Figure V.10. *Drain current density as a function of gate length for varying thicknesses (W_g = 10 nm and 20 nm); (a) On-state current (I_{on}) and (b) Off-state current (I_{off}).*

In field-effect transistors, including MOSFETs, CNTFETs, and GNRFETs, trans-conductance (g_m) serves as a key metric representing the device's capability to regulate the drain current by modulating the gate-source voltage. Elevated values of g_m signify enhanced control over the current, which is essential for effectively amplifying variations in the drain current, particularly when the device is exposed to external stimuli such as ammonia gas. As shown in **Figure** V.**11**, an increase in the dielectric constant results in a significant rise in the ON-state current, which in turn boosts the transconductance (g_m). $LaAlO_3$ was chosen as the gate dielectric because of its excellent interface compatibility with graphene, creating a clean and sharp interface that reduces charge trapping and maintains the high carrier mobility of graphene [45]. In comparison to HfO_2 and Al_2O_3, $LaAlO_3$ demonstrates superior dielectric robustness, owing to its notably high dielectric constant (approximately 30), a more substantial band offset with graphene, and exceptional breakdown resilience. These attributes collectively contribute to its enhanced reliability as a gate dielectric material [46],[47]. Experimental studies reveal that graphene FETs incorporating $LaAlO_3$ exhibit superior performance metrics, including higher on/off current ratios, more favorable subthreshold swings, and improved thermal stability when compared to devices utilizing HfO_2 or Al_2O_3 as gate dielectrics [46,48].

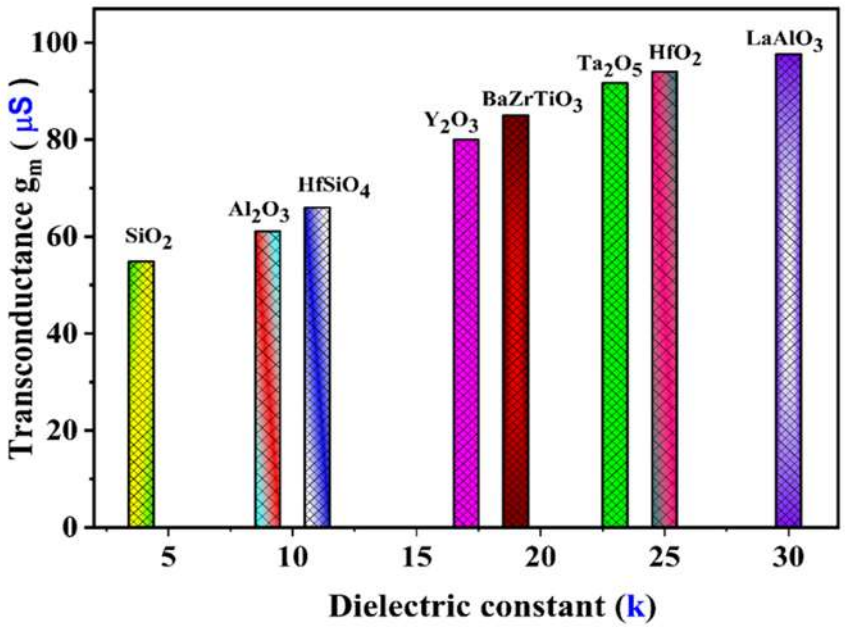


***Figure** V.11. Transconductance (g_m) as a function of the dielectric constant (k) measured at V_{DS} = 0.4 V and V_{GS} = 0.7 V.*

$LaAlO_3$ enables an ultrathin equivalent oxide thickness (EOT) as low as 0.31 nm without the formation of an interfacial SiO_2 layer, a common issue with HfO_2 and Al_2O_3. This direct $LaAlO_3$/Si interface significantly reduces interface trap densities and enhances thermal stability by suppressing the growth of interfacial layers that typically degrade device performance. Leakage current assessments reveal that $LaAlO_3$ gate stacks exhibit leakage currents at least an order of magnitude lower than those of Hf-based dielectrics with comparable EOTs, and up to six orders of magnitude lower than SiO_2. This improvement is attributed to larger conduction and valence band offsets ($\Delta Ec \approx 1.9$ eV, $\Delta Ev \approx 2.2$ eV), which effectively inhibit carrier tunneling. Furthermore, $LaAlO_3$ shows exceptional thermal stability, facilitating low-temperature fabrication processes compatible with advanced device architectures without compromising dielectric integrity. In contrast, HfO_2 and Al_2O_3 typically require additional passivation layers to mitigate interface traps, suffer from higher leakage currents, and exhibit less stable effective work functions under thermal annealing. $LaAlO_3$'s stable effective work function, coupled with tunable threshold voltage via adjustment of the La/(La+Al) ratio, provides enhanced flexibility in device design.

Collectively, $LaAlO_3$ outperforms HfO_2 and Al_2O_3 by offering superior interface quality, significantly reduced leakage, higher dielectric constant, and improved thermal stability, establishing it as the preferred high-k dielectric for high-performance, scaled CMOS

applications [49–56]. Theoretical analyses further validate that $LaAlO_3$ maintains the intrinsic linear Dirac cone dispersion of graphene with negligible disturbance, in contrast to certain other dielectric materials that can cause bandgap opening or Fermi level pinning, thereby compromising device performance [57].

The combination of these benefits positions $LaAlO_3$ as the ideal dielectric for our research. Employing lanthanum aluminate ($LaAlO_3$) as the gate dielectric in graphene nanoribbon field-effect transistors (GNRFETs) significantly enhances transconductance, reaching 88.5 μS. Conversely, using silicon dioxide (SiO_2) for the gate dielectric results in a lower transconductance of 55 μS. Comparisons across various dielectric materials emphasize the critical influence of dielectric selection on optimizing GNRFET performance, particularly regarding transconductive efficiency. A higher dielectric constant increases the gate capacitance, which subsequently elevates the transconductance. This enhancement translates to a greater variation in drain current in response to changes in gate voltage, thereby boosting the sensor's ability to detect alterations in channel conductance caused by gas adsorption [58,59]. Every parameter analyzed in this research was meticulously selected due to its substantial effect on the performance and characteristics of GNRFET gas sensors.

V.6.1 Assessment of Practical Feasibility, Experimental Validation, and Benchmarking of I-V Characteristics

Although this study primarily centers on theoretical modeling and simulation, the practical feasibility of fabricating the proposed GNRFET structures must also be acknowledged. Recent progress in nanofabrication techniques has proven the capability to produce graphene nanoribbon field effect transistors with channel lengths under 20 nm, alongside the successful integration of high-K dielectrics like $LaAlO_3$ [60-62]. Methods such as bottom-up synthesis, transfer-free integration, and cutting-edge lithography have facilitated the fabrication of GNRFETs that exhibit outstanding electrical performance and scalability [61,63].

In a notable study, Wang et al. (2009) [56] achieved the fabrication of sub-10-nm all-semiconducting graphene nanoribbon FETs, exhibiting high on/off ratios and stable operation at room temperature. Likewise, Cai et al. (2010) [61] and Kolmer et al. (2020) [62] successfully synthesized graphene nanoribbons with atomic precision and demonstrated their incorporation into devices suitable for large-scale production. These experimental outcomes closely align with the theoretical device parameters and performance metrics presented in our analysis.

Furthermore, the integration of high-K dielectrics, including $LaAlO_3$, confirms the practical applicability and scalable potential of our proposed sensor design [64,65]. Therefore, our results demonstrate both strong theoretical validity and practical feasibility, laying a solid foundation for the advancement of high-performance GNRFET-based sensors. To ensure the precision and reliability of our GNRFET gas sensor model, especially regarding its current-voltage (I-V) behavior, we conducted a comprehensive benchmarking of our simulation outcomes against established experimental data and state of the art simulation studies reported in the literature.

Mahmoudi et al. [35] conducted comprehensive simulations of GNRFET gas sensors subjected to ammonia, utilizing a model that integrates the Poisson equation and quantum transport phenomena to analyze output I-V characteristics. Their findings indicated a sensitivity of around 2.7% at 1 ppm NH_3 concentration, with noticeable changes in the drain current upon exposure to the gas. Our simulation results exhibit consistent behavior, showing comparable shifts in the I-V curves in response to different ammonia concentrations, thereby validating the model's effectiveness in capturing the fundamental sensing mechanisms. Additionally, Kheirabadi et al. [66] conducted experimental research on bilayer armchair graphene nanoribbons, demonstrating selective gas sensing through conductance variations associated with gas adsorption. While their study targeted different gases, the observed alterations in electronic transport qualitatively correspond with the shifts in I-V characteristics we report under ammonia exposure. Furthermore, Rashid M.H. et al. [67] performed simulations on GNRFET devices subjected to different gate voltages and gas molecule adsorption, demonstrating that target gas presence causes notable changes in the I-V characteristics through charge transfer mechanisms.

This finding reinforces our methodology of incorporating gate voltage-dependent current modulation to improve sensor selectivity and sensitivity. Significantly, the double-gate GNRFET configuration analyzed by Tamersit et al. [58] through the nonequilibrium Green function (NEGF) approach revealed that sensor operation within the subthreshold regime optimizes sensitivity, marked by pronounced variations in I-V characteristics following gas adsorption. Our model concurs, forecasting greater sensitivity and more distinct I-V modulation in this regime, thereby supporting the selection of the device architecture and operating parameters. Experimentally, Song et al. demonstrated that vertical graphene field-effect transistors (VGr-FETs) display substantial I-V modulation upon exposure to ammonia, achieving detection limits down to 86 ppb and on/off current ratios reaching 10^3.

Although the device designs differ, the fundamental mechanism of current modulation induced by adsorbed gas molecules aligns with our GNRFET model, further affirming its practical applicability. Significantly, the double-gate GNRFET structure examined by [58] using the nonequilibrium Green function (NEGF) method showed that operating the sensor in the subthreshold region enhances sensitivity, with notable changes in I-V characteristics upon gas adsorption. Our model similarly predicts increased sensitivity and more distinct I-V modulation in this regime, supporting the chosen device design and operational conditions. On the experimental side, vertical graphene field-effect transistors (VGr-FETs) studied by Song et al. [68] demonstrated considerable I-V modulation in response to ammonia exposure, with detection limits as low as 86 ppb and on/off current ratios up to 10^3. Despite differences in device architecture, the fundamental mechanism of current modulation by adsorbed gas molecules aligns closely with our GNRFET model, reinforcing its practical relevance.

Together, these experimental and simulation benchmarks demonstrate that our GNRFET gas sensor model reliably replicates the essential I-V characteristic behaviors seen in cutting-edge devices. This validation underscores the model's effectiveness for guiding sensor design optimization and accurately forecasting performance across different gas concentrations and operational settings.

V.7. Conclusion

In this chapter, we have established a comprehensive simulation framework grounded in a robust analytical model implemented in MATLAB to elucidate the current-voltage (I–V) characteristics of graphene nanoribbon field-effect transistors (GNRFETs). The analysis reveals a substantial modulation of the drain current upon exposure to ammonia (NH_3), exhibiting an increase by two orders of magnitude from 10^{-7} A to 10^{-5} A at a concentration of 300 ppm. This marked enhancement decisively demonstrates the high sensitivity of GNRFETs to NH_3, highlighting their promise as advanced platforms for gas sensing applications. The findings deepen the understanding of charge transfer interactions governing device response, thereby providing a solid foundation for the rational design and optimization of graphene-based sensors tailored for environmental and industrial monitoring. A systematic investigation was conducted to assess the influence of key parameters, including temperature, gate length, and dual oxide layer thickness, on critical device performance metrics. The results establish a direct correlation between drain current (I_{ds}) and both top gate oxide thickness and ambient temperature, contrasted by an inverse dependence on channel length and back gate oxide thickness. Furthermore, the study underscores the pronounced effect of graphene nanoribbon width

(examined at 10 nm and 20 nm) on the electronic properties, attributable to quantum confinement phenomena. By integrating lanthanum aluminate ($LaAlO_3$) as the gate dielectric, the work identifies pivotal correlations that enhance the understanding of drain current sensitivity, thereby guiding the advancement of GNRFET architectures for enhanced gas detection capabilities.

This research contributes critical insights and practical design considerations for the enhancement of graphene nanoribbon FET configurations, reinforcing their potential integration within sophisticated electronic sensing systems. The outcomes enrich the broader gas sensor research domain and set the stage for subsequent innovations in highly sensitive and efficient detection technologies. Recognizing the importance of device stability and operational longevity, future efforts will focus on investigating the effects of prolonged ammonia exposure and various doping methodologies on GNRFET performance. Additionally, forthcoming studies will explore the impacts of thermal noise and scattering mechanisms, which are essential for optimizing device functionality and further elevating sensor sensitivity. These investigations will be detailed in subsequent publications.

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General Conclusion

General Conclusion

This thesis has delivered an extensive and systematic exploration of nano-carbon transistor technologies, focusing primarily on carbon nanotube (CNT) and graphene nanoribbon (GNR) field-effect transistors (FETs). These devices represent forefront alternatives to conventional silicon-based transistors, whose scaling limits have motivated the search for innovative nanoelectronics materials and architectures capable of meeting the increasing demands for performance, energy efficiency, and multifunctionality. The foundational material science underpinning this research was established through an in-depth review of carbon allotropes, highlighting the atomic hybridization, structural configurations, and synthesis techniques that govern the intrinsic electronic and physical properties of CNTs and GNR.

The overarching problem addressed in this study involves understanding and harnessing the effects of external stimuli namely, optical excitation and chemical gas exposure on the electrical characteristics and transport mechanisms of carbon-based FET devices. Specifically, the work investigates how optical gating modifies the current-voltage (I–V) behavior of optical gated CNTFETs (OG-CNTFETs) and how exposure to ammonia (NH_3) gas impacts the electrical response of double-gated graphene nanoribbon FETs (DG-GNRFETs) employing $LaAlO_3$ as a high-k gate dielectric. Tackling this problem is vital to enabling advanced functionalities such as optoelectronic switching and highly sensitive gas sensing within integrated nanoelectronics platforms.

Methodologically, the thesis advanced the field by developing and applying detailed modeling and simulation frameworks to characterize device-level responses under combined electrical, optical, and chemical inputs. For OG-CNTFETs, the research quantified the interplay between photogenerated carrier dynamics and electrostatic channel modulation, illuminating parameters that govern reversible tuning of transport characteristics via optical stimuli. This analysis revealed critical dependencies on illumination power, wavelength, and device geometry, providing guidelines for optimizing photo response and enhancing device sensitivity for potential applications in photodetection and reconfigurable logic circuits. Concurrently, the DG-GNRFET study elucidated how the dual-gate configuration and $LaAlO_3$ dielectric enhance electrostatic control, thereby improving sensor responsiveness to NH_3 gas adsorption. Investigations into the effects of gate voltage, dielectric thickness, and gas concentration shed light on the modulation of drain current, I_{on}/I_{off} ratio, and transconductance, validating the

device design as a promising platform for nanoscale chemical sensing with improved selectivity and stability.

The results obtained are significant both conceptually and practically. Demonstrating the feasibility of optical control in CNTFETs expands the functional repertoire of carbon-based nanoscale transistors beyond traditional electrical gating, paving the way toward hybrid optoelectronic devices that integrate light and charge modulation in a single platform. This capability not only broadens device applicability but also introduces novel mechanisms for signal processing and sensing in nanosystems. On the gas sensing front, the improved sensitivity and selectivity achieved in DG-GNRFETs using $LaAlO_3$ underscores the critical role of dielectric engineering and multi-gate architectures in enhancing environmental sensor performance at the nanoscale. These findings have meaningful implications for the design of future compact, efficient, and selective chemical sensors necessary for real-time environmental monitoring.

Beyond the immediate outcomes, this thesis contributes to the overarching goal of bridging fundamental material knowledge and device engineering of nano-carbon FETs, fostering their translation from laboratory prototypes to practical applications. The incorporation of detailed electrostatic modeling and simulation frameworks equips researchers with tools to predict and optimize device operation under multi-physical stimuli, which is essential for tailoring performance to specific applications.

Looking ahead, several crucial research directions emerge from this work. A foremost challenge remains the refinement of synthesis and fabrication techniques for CNTs and GNRs to achieve uniform, reproducible, and scalable production with controlled chirality, width, and edge structure, addressing fundamental bottlenecks in device uniformity and yiel. Additionally, advancing the understanding of interface phenomena particularly under simultaneous optical and chemical influences will be vital to improve device stability, reliability, and sensitivity. The complexity of charge trapping, surface states, and dielectric interactions at nanoscale interfaces demands further experimental characterization and theoretical modeling to inform device optimization strategies. Moreover, integrating these nano-carbon transistors into complex circuits and heterogeneous systems represents a critical step for their practical deployment. Future studies should emphasize device-to-device variability, compatibility with established CMOS fabrication processes, and system-level modeling to enable seamless incorporation into multifunctional electronics, including flexible and wearable technologie. The exploration of

hybrid device concepts that combine optical, electrical, and chemical functionalities holds promise for revolutionary applications in sensing, communication, and logic.

In conclusion, this thesis establishes a substantial foundation for the development and application of carbon nanotube and graphene nanoribbon FETs in advanced nanoelectronic devices. By thoroughly articulating the material science principles, device physics, and multifunctional operation of OG-CNTFETs and DG-GNRFETs, the research delivers valuable conceptual and methodological advances to the field of carbon nanoelectronics. The insights gained highlight the transformative potential of nano-carbon transistors to surpass silicon-based limitations and enable new paradigms in electronic device design. This work thus contributes meaningfully to the ongoing progress toward faster, smaller, and more versatile electronic systems tailored for the technological challenges of the future.

Abstract

This thesis presents a comprehensive study of nano-carbon transistors based on carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), focusing on their synthesis, fundamental electronic properties, and device architectures. It begins with an overview of carbon allotropes, highlighting the effects of material structure on electronic behavior. The work then reviews field-effect transistor (FET) fundamentals, progressing from conventional MOSFETs to various CNTFETs, with particular attention to optically gated CNTFETs and their potential in optoelectronic applications. Subsequently, the study explores the fabrication and operation of graphene nanoribbon FETs (GNRFETs), emphasizing their use in gas sensing. Through simulation, optical gating effects on CNTFET I–V characteristics and photocurrent generation are characterized. An applied investigation focuses on double-gated GNRFET gas sensors using $LaAlO_3$ gate dielectrics, analyzing sensor response to ammonia NH_3 exposure and the influence of parameters such as voltage, dielectric properties, and gas concentration on performance metrics. This research advances the understanding of nano-carbon device physics and applications for future nanoelectronic and sensing platforms.

Keywords : carbon nanotubes (CNT), graphene nanoribbons (GNR), field-effect transistors (FET), OG-CNTFET, GNRFETgas sensor, $LaAlO_3$ dielectric, NH_3.

Résumé

Cette thèse présente une étude complète des transistors à nano-carbone basés sur les nanotubes de carbone (CNT) et les nanorubans de graphène (GNR), en se concentrant sur leur synthèse, leurs propriétés électroniques fondamentales et leurs architectures de dispositifs. Elle débute par un aperçu des allotropes du carbone, mettant en lumière l'impact de la structure matérielle sur le comportement électronique. Le travail passe ensuite en revue les principes du transistor à effet de champ (FET), évoluant des MOSFET classiques vers diverses configurations de CNTFET, avec une attention particulière aux CNTFET à commande optique et leur potentiel pour des applications optoélectroniques. Par la suite, l'étude explore la fabrication et le fonctionnement des transistors à nanoruban de graphène (GNRFET), en insistant sur leur utilisation dans la détection de gaz. À travers des simulations, les effets du contrôle optique sur les caractéristiques I–V des CNTFET et la génération de photo courant sont caractérisés. Une étude appliquée se concentre sur des capteurs à base de GNRFET à double grille utilisant un diélectrique $LaAlO_3$, analysant la réponse du capteur à l'exposition à l'ammoniac NH_3 et l'influence de paramètres tels que la tension, les propriétés du diélectrique et la concentration de gaz sur les performances. Cette recherche approfondit la compréhension de la physique des dispositifs nano-carbone et de leurs applications pour les futures plateformes nanoélectroniques et de détection.

Mots-clés : nanotubes de carbone (CNT), nanorubans de graphène (GNR), transistors à effet de champ (FET), OG-CNTFET, DG-GNRFET, $LaAlO_3$, caractéristiques I–V, NH_3.

ملخص

تقدم هذه الأطروحة دراسة شاملة لأشباه الموصلات النانوية القائمة على أنابيب الكربون النانوية (CNT) وأشرطة الجرافين النانوية (GNR)، مع التركيز على طرق تصنيعها وخصائصها الإلكترونية الأساسية وهندسة أجهزتها. تبدأ الأطروحة بمراجعة أنماط الترتيب الذري للكربون، مع إبراز تأثير بنية المادة على السلوك الإلكتروني. ثم تستعرض مبادئ الترانزستورات ذات التأثير الحقل (FET) بدءًا من الترانزستورات التقليدية (MOSFET) وصولًا إلى أنواع متعددة من CNTFET، مع تركيز خاص على الترانزستورات ذات البوابة الضوئية وإمكاناتها في التطبيقات البصرية الإلكترونية. بعد ذلك، تتناول الدراسة تصنيع وتشغيل ترانزستورات أشرطة الجرافين (GNRFET) مع تسليط الضوء على تطبيقاتها في استشعار الغازات. من خلال المحاكاة، توضح الأطروحة تأثير التحكم الضوئي على خصائص التيار-الجهد (I–V) في CNTFET وآليات توليد التيار الضوئي. تركز الدراسة التطبيقية على حساسات غاز مبنية على GNRFET مزدوجة البوابة مع عازل $LaAlO_3$، وتحلل استجابة الحساس لتعرض الأمونيا NH_3وتأثير متغيرات مثل الجهد وخصائص العازل وتركيز الغاز على أداء الحساس. تعزز هذه البحث الفهم العلمي لأجهزة النانو الكربونية وتطبيقاتها في منصات النانوإلكترونيات والاستشعار المستقبلية.

الكلمات المفتاحية: أنابيب الكربون النانوية CNT، أشرطة الجرافين النانوية GNR، ترانزستورات التأثير الحقلية FET، OG-CNTFET، حساسات الغازات GNRFET، عازل $LaAlO_3$، خصائص التيار-الجهد(I–V) ، الأمونيا NH_3