Abbes Laghrour University, Khenchela

First-year Mathematics — Year 2024/2025
Machine Structure 2 — 1h :30

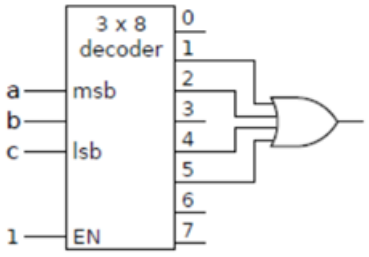
Model answer

Exercise 1 (06 pts)

Consider the Boolean function : $a\overline{b} + \overline{b}c + \overline{a}b\overline{c}$

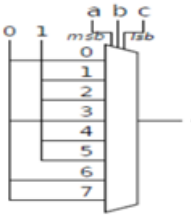
1. Use a 3 x 8 decoder plus whatever logic gates are needed to implement this function.

   For a decoder implementation one must identify the minterms. One easy way to do that is to construct a truth table. The minterms are m1, m2, m4, and m5. Since there are three variables (a, b, and c) a 3 Œ 8 decoder is needed. The decoder outputs corresponding to these minterms are connected to an OR gate, as is done in the diagram



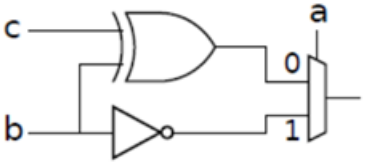
2. Use an 8-input multiplexer to implement this function (Do not use any gate).

   As with the decoder, minterms are used. Set the multiplexer inputs corresponding to the minterms to 1, and set the other inputs to 0. The select inputs are connected to the variables.



3. Use a multiplexer (2x1) and additional logic, including an exclusive-or gate, (Hint : use ń a ż as the multiplexer control input).

   it might be easier to eyeball a truth table than to do this by algebraic manipulation. Implement using a multiplexer based on a. When a = 0 the function is $\overline{b}c + b\overline{c} = b \oplus c$. When a = 1 the function is $\overline{b} + \overline{b}c = b$. These two expressions are used for the multiplexer inputs as is done in the diagram.



Exercise 2 (04 pts)

Full adder.

Exercice 3 (10 pts)

A 4-bit Serial-In Parallel-Out (SIPO) shift register is initially loaded with the value 1111. A data sequence 1010 is applied to the serial input.

1. What will be the parallel output of the register after 3 clock cycles ?

Cycle	**Serial Input**	**Register State (Q3 Q2 Q1 Q0)**
Initial		1 1 1 1
1	0	0 1 1 1
2	1	1 0 1 1
3	0	0 1 0 1

TABLE 1 – Évolution du registre à chaque cycle

2. Draw the timing diagram showing the clock signal, the serial input signal, and the evolution of the 4-bit parallel output over the first 4 clock cycles.