Abbes Laghrour University, Khenchela

First-year Mathematics — Year 2024/2025
Machine Structure 2 — 1h :30

Final Exam

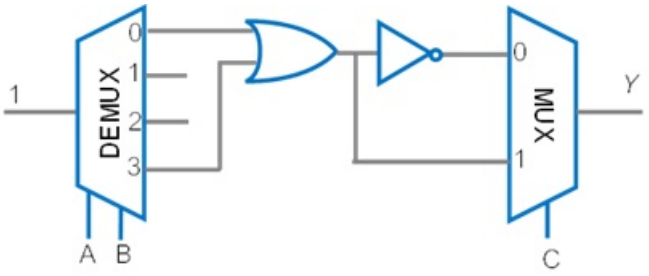
Exercise 1 (06 pts)

Consider the Boolean function : $f = a\overline{b} + \overline{b}c + \overline{a}b\overline{c}$

1. Use a 3 x 8 decoder plus whatever logic gates are needed to implement this function.
2. Use an 8-input multiplexer to implement this function (Do not use any gate).
3. Use a 2x1 multiplexer along with an exclusive-OR gate and a NOT gate. Use a as the selection line for the multiplexer.

Exercise 2 (04 pts)

What is the function of this circuit



Exercice 3 (10 pts)

A 4-bit Serial-In Parallel-Out (SIPO) shift register is initially loaded with the value 1111. A data sequence 1010 is applied to the serial input.

1. What will be the parallel output of the register after 3 clock cycles ?
2. Draw the timing diagram showing the clock signal, the serial input signal, and the evolution of the 4-bit parallel output (Q3 Q2 Q1 Q0) over the first 4 clock cycles(rising edge).

Good luck !